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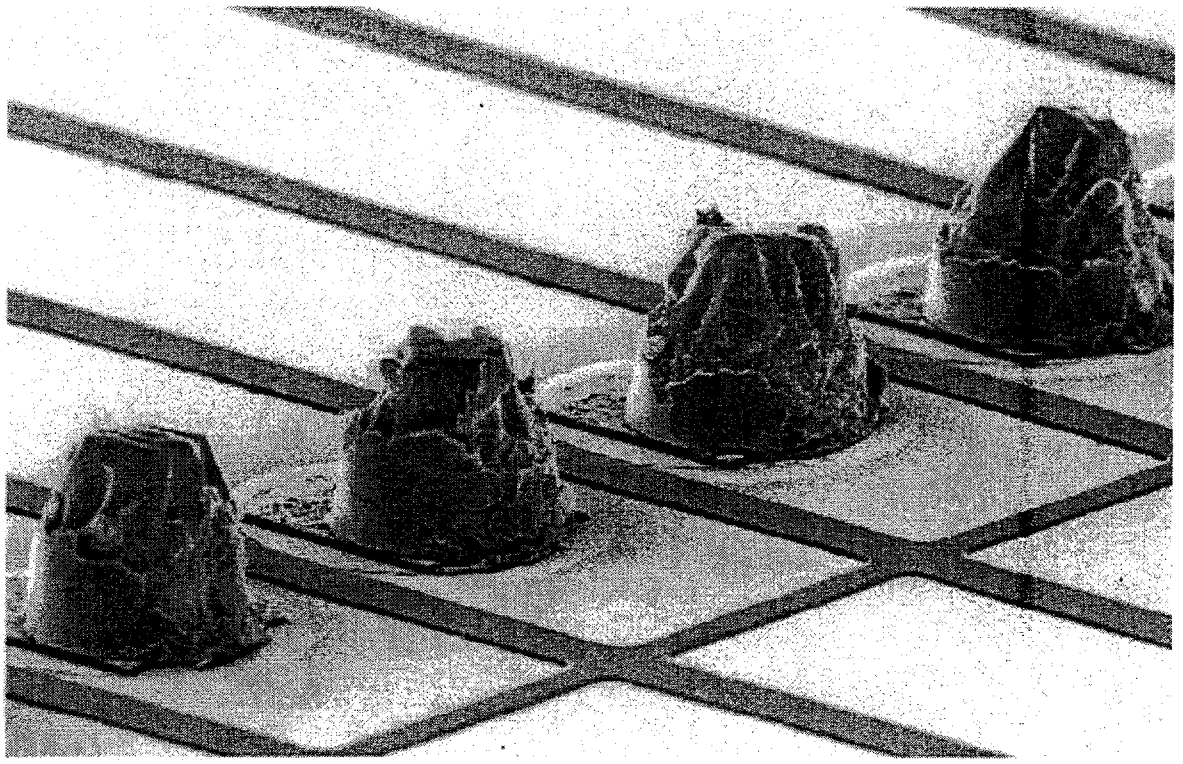
Proceedings of PIXEL98 - International Pixel Detector Workshop



May 7-9, 1998
Fermi National Accelerator Laboratory
Batavia, Illinois

Editors
David F. Anderson
Simon Kwan

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Distribution

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Preface

Experiments around the globe face new challenges of more precision in the face of higher interaction rates, greater track densities, and higher radiation doses, as they look for rarer and rarer processes, leading many to incorporate pixelated solid-state detectors into their plans. The highest-readout-rate devices require new technologies for implementation. The PIXEL98 Workshop (Fermilab, May 7-9, 1998) reviewed recent, significant progress in meeting these technical challenges. Participants presented many new results; many of them from the weeks – even days – just before the workshop.

Brand new at this workshop were results on cryogenic operation of radiation-damaged silicon detectors (dubbed "the Lazarus effect"). Other new work included a diamond sensor with 280-micron collection distance); new results on breakdown in p-type silicon detectors); testing of the latest versions of read-out chip and interconnection designs; and the radiation hardness of deep-submicron processes.

Approximately 100 attendees from all the major high-energy physics efforts throughout the world, over half from non-U.S. institutions, came to Fermilab for the meeting. Simon Kwan of Fermilab chaired the international and local organizing committees for the workshop.

Given the scale of the detector systems and the technologies involved, solving the technical problems requires close collaboration with industry. Finding solutions for bump-bonding (the assembly of readout chips to sensors), multiple chip assembly, radiation-hard electronics, and advanced material use all require joint industry-laboratory effort. Thus, the active participation of industry, particularly with bump-bonding/flip-chip capability, was a highlight of the workshop. The vendors participated in the formal presentations and in a less formal poster session and reception on the workshop's first evening.

Despite differences in physics goals and experiment environments among participants, the themes of precision spatial resolution, two-dimensional information for pattern recognition, high radiation tolerance, large amounts of data, and low mass emerged as key factors.

Two groups with experience running large scale tracking systems of silicon pixels (DELPHI and WA97/NA57), four groups planning to use large tracking systems (ATLAS, CMS, ALICE, and BTeV), and one group planning to use pixel detectors in hybrid photon detectors (LHCb RICH) gave presentations in a systems requirements session. The extremely clean Omega signal, extracted by WA97 without kaon identification from events often containing more than 50 tracks reconstructed in a 5 cm x 5 cm telescope, provided a dramatic demonstration of the pattern recognition power of pixel detectors.

The full-to-bursting session on readout electronics included ten presentations. Most of the talks described progress made by groups designing readout systems for the LHC experiments. There, the pixel detectors and readout schemes are very different: rectangular pixels vs. square pixels; "binary" vs. "digital" vs. "analog" readout. CMS also plans to use an (octal) analog encoding scheme to reduce the pin count and number of bus lines required to transmit inherently digital information, such as pixel addresses. However, some similarities are emerging, notably leakage-current tolerance provided by a nonlinear, synthetic resistor in the preamplifier feedback circuit and the use of a three-bit DAC to provide cell-to-cell discriminator threshold trimming. Much of the hallway conversation outside the meeting room focused on the possibility that standard CMOS processes with "deep submicron" (0.25 micron and below) feature size may be inherently radiation hard; and on the continued mystery of the increased noise seen by many groups after bump bonding.

A session on detectors focused on radiation damage and techniques to mitigate its effects. An overview of the physics of radiation damage in silicon detectors by Zheng Li (BNL) opened the session. Vittorio Palmieri (Bern) presented just-completed work on the

resurrected operation at cryogenic temperatures of very radiation-damaged silicon detectors (the Lazarus effect) and on the cryogenic operation of silicon as an ionization chamber with ohmic contacts. William Trischuk (Toronto) presented results on a diamond sensor with 280 micron collection distance, a new record, and a bump-bonded diamond pixel detector. New work was also presented on p-type silicon detectors (Gino Bolla, Purdue), and on progress on the first fabrication run of 3-dimension detectors by Sherwood Parker (Hawaii). The meeting highlighted the differences in guard-ring structures in the CMS and ATLAS prototypes.

The session on bump-bonding included presentations from four vendors. These talks covered the basics of bump bonding, techniques used, pros and cons of indium versus lead-tin solder, flip-chip mating, and results on failure rate. Results from ATLAS and CMS on the yield rate for their prototype module assembly studies were also presented.

An interconnection and data readout session featured talks from ATLAS, CDF and CMS. The talks ranged from flexible circuit and optical data transmission technology developments (Mark Bailey of New Mexico and Pat Skubic of Oklahoma on the first of these, and Yi-Cheng Liu of Academia Sinica on the second) to control circuits (Robert Stone of Rutgers). The results for multilayer circuits on flexible plastics, in particular, showed new successes. Peter Gerlach (Wuppertal) described the unique ATLAS plan for combining some of the flexible-circuit and control-chip functions.

The infrastructure session focused on the fabrication, design, and cooling of the ALICE, ATLAS, and CMS pixel detectors. A number of talks featured the use of light-weight carbon composite materials for structure and cooling. Work on evaporative cooling for ATLAS is well advanced and looks promising. The close of the session featured a comprehensive presentation of the alignment and performance of the SLD CCD pixel detector by Glen Crawford (SLAC).

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Pixel 98

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Construction and Performance of the WA97/NA57 Silicon Pixel Telescope

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Abstract

The silicon pixel telescope installed in WA97 has gradually upgraded from the first 72k pixel plane tested in 1993 to the present 13 planes telescope, which was successfully commissioned in the first run of NA57 (1997).

This 1.1 million channel detector is described along with some of its important characteristics, such as the spatial resolution (~12um) and the time resolution (16ns r.m.s for the Omega3 planes). Special emphasis will be put on the construction of the telescope and on how various procedures and systems ensured reliable operation of this detector.

In the high track multiplicity environment of central Pb-Pb interactions, where any other kind of detector would fail, the pixel telescope provided in the last four years of runs the precise measurements needed to achieve the physics goals of the WA97 experiment.

Introduction

The WA97 [1] and NA57 [2] experiments study strange and multi-strange baryon and anti-baryon production in central Pb-Pb collisions at CERN SPS. The extremely high multiplicity of such events yields a large number of simultaneous hits in the sensitive apparatus (fig.1). Pixel detectors were chosen as tracking devices in this environment for their high spatial resolution and their unambiguous two-dimensional information [3].

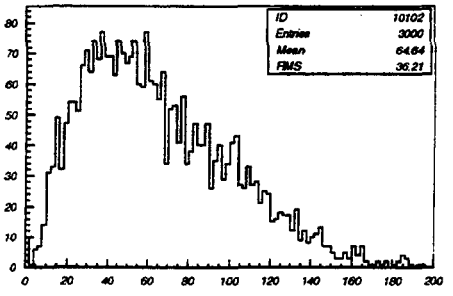

Fig.1: Multiplicity distribution in an Ω3 plane during the 1996 WA97 Pb run

System description

The "Omega2" and "Omega3" silicon pixel detector systems were developed with the effective support of the CERN RD19 collaboration to equip the tracking telescope. In both systems 6 integrated front-end/read-out chips are bump bonded to a silicon detector segmented in pixels. Several of these modules, called "ladders" are assembled on a thin ceramic carrier to form an "array". Two arrays, suitably staggered, cover hermetically an area of 5×5 cm^2 and form a "plane". The tracking telescope is built from several planes aligned one after the other on a mechanical frame.

In the Omega2 system the pixel size is 75×500μm^2, and each pixel electronic cell contains a charge preamplifier, a discriminator with adjustable threshold, a delay element and a coincidence unit. The output is recorded in a flip-flop that can be read out through a shift register [4]. Each Omega2 front-end/read-out chip contains 1006 sensitive cells and 16 cells connected to an electric test input.

The Omega3 chip consists of 2032 sensitive cells sized 50×500μm^2. Two flip-flops per cell allow to test and mask each channel individually, so that Omega3 chips can be fully tested at the wafer level. Three additional bits per pixel control a tunable delay line that can be used to finely adjust the timing of the different cells [5]. Thanks to the introduction of this distributed digital control a very accurate time resolution (6ns r.m.s. after tuning the delay lines) was achieved with the Ω3 chips [6].

The carrier on which Ω3 ladders are assembled is manufactured on a ceramic support and consists of five conductive Al layers separated by Al_2O_3 dielectric. Its overall thickness is about 400μm. The carrier was designed in order to provide good decoupling and low impedance connection to the power supplies [7].

The telescope which was successfully commissioned in the 1997 proton run of NA57 consists of seven Ω2 and six Ω3 planes, for a total of 1 092 240 channels. It contains 84 Ω2 ladders, coupled to 504 readout chips and 48 Ω3 ladders, bonded to 288 readout chips.

Each array in the telescope is read out by a VME system, consisting of two PCBs equipped with programmable logic (LCAs) and standard CMOS and TTL ICs. One card, the "motherboard", is directly connected to the array, via a flexible epoxy PCB. The

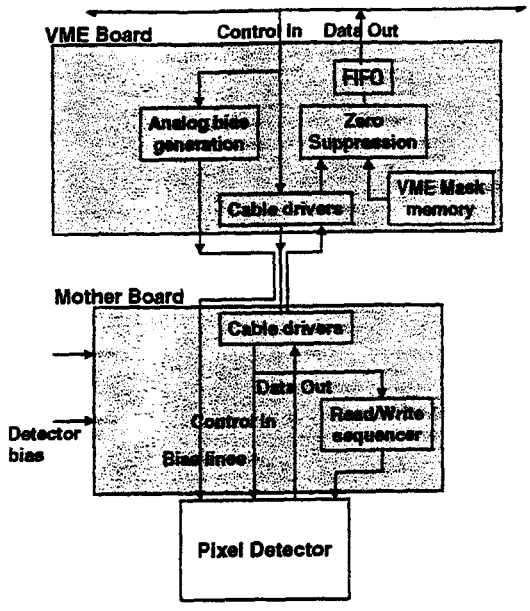

Fig.2: Block diagram of the Ω3 VME system

motherboard is then connected to the VME card, located in the control room, through a 30m 100 twisted pair cable. A block diagram explaining the functions of both cards is shown in fig.2.

The Ω3 VME system provides a bi-directional link between the VME bus and the pixel array. This allows to download the values of the different control registers in the pixel chips and to read out the data coming from the detector.

The readout frequency is 4MHz, due to the low speed of the programmable logic. Two chips are read out in parallel to form a 32bit data word which complies with the VME standard. Each card can read an array (49 152 pixels) in ~400μsec, suppressing the words that contain only zeros. A FIFO provides a buffer between the detector system and the VME bus.

A second level of masking and 5 DACs which provide the analogue bias currents for the integrated electronics are also included in the VME board.

To ensure reliable operation of the telescope during data taking, a cooling and a slow control system were also designed and implemented inside the NA57 spectrometer.

We observed that local heating of the detector by the integrated readout electronics can cause a significant rise in the leakage current. This increases electronics noise, so that more channels become permanently active and the temperature tends to rise further. This dangerous thermal runaway can effectively be counteracted by cooling the detectors. A simple scheme, in which each Ω3 plane is fluxed with ~10l/h of 5-10°C N_2 proved to be effective in reducing the frequency of the runaway (which was observed only once in the week of commissioning run of NA57).

The slow control system (fig. 3) provides the detectors bias for all the planes and the power supply for the Ω3 integrated electronics [8]. All leakage currents and the power consumption of the Ω3 arrays are constantly monitored. If any of the currents exceeds its preset value, the array affected by the fault is switched off and an alarm is sent to the shifter, who can start an automatic recovery procedure, or call the expert.

A graphic interface developed under Labview provides an easy way to check all the parameters, to keep a logbook of their history and to change the defaults.

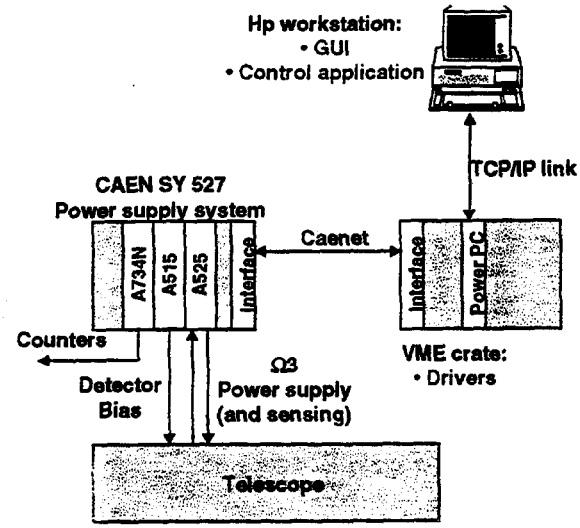

Fig.3: Block diagram of the NA57 slow control system

Telescope production

Several phases of manufacturing and testing have to be properly performed in order to produce the pixel detectors used in WA97/NA57.

Ω3 chips are tested at wafer level by means of a fully automated tester developed "in house". This system integrates a VME processor, the Ω3 VME readout, an automatic probe station controlled via GPIB, a set of DACs and ADCs and a CAMAC Programmable Delay Generator [9]. It is able of running a full functional test of the Ω3 chip in ~100s , checking the following parameters:

- value of the analogue bias currents
- functionality of all control registers
- tristate operation of the output buffers
- response of the front end to the electrical test
- number of "blinking"[1] pixels
- minimum and maximum internal delay

[1] Pixels that exhibit a non-poisson noise distribution and have to be masked during normal detector operation are referred to as "blinking"

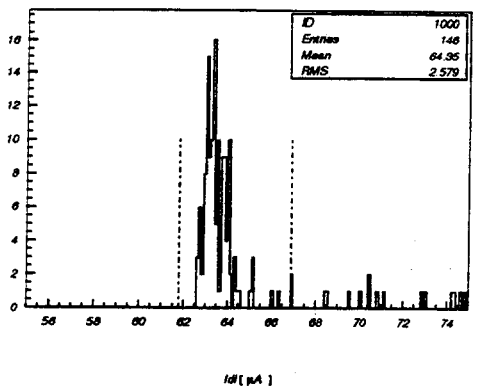

Fig. 4: Distribution of the delay control current (Idl) on one Ω3 wafer

In order to pass the test each chip must have perfect digital and I/O functionality, fewer than 128 pixels not responding to the test pulse and fewer than 300 blinking pixels. Moreover, all the analogue bias currents have to stay within one σ from the mean value measured on the whole wafer.

Figure 4 shows, for example, the distribution of the delay control current on a Ω3 wafer [9]. The lines represent the one σ cut level.

Known good die are flip-chip bonded by means of Sn-Pb solder bumps to the detector ladders [10].

The quality of the bump bonding is checked by means of a second probe test. The detector on top of each chip is exposed to a Sr^{90} source and 0.5 to 1×10^6 random triggers are recorded, in order to produce a source profile. Fig. 5 shows the results of such a test on a Ω3 ladder: the six chips and the shadow of the needle used to bias the detector backplane are clearly visible. Only detectors with a bonding yield better than 95% are selected for assembling onto the ceramic carrier.

The completed array undergoes a severe final test. All chip registers are tested again, blinking pixels are located and masked and a VME level mask is also generated. The threshold of each pixel is estimated electrically [6] and the bias currents are tuned to ensure 100% particle detection efficiency for a 300μm detector (max. threshold <9000e⁻ [11], [12]). The array is exposed to a Sr^{90} source to check the bump bonding quality after the mechanical and thermal stresses induced by manufacturing. Fig.6 shows the source profile recorded on a Ω3 array with very good bonding yield. The delay of each pixel is finally tuned in order to optimise time resolution [6].

Telescope performance

After masking blinking pixels the spurious hit rate of the Ω2 part of the telescope measured in the WA97

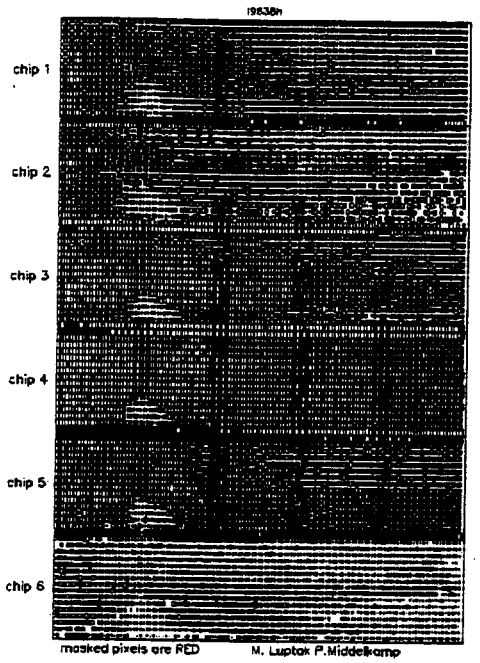

Fig.5: Ladder test with a Sr^{90} source. Chips are contacted one a time for the test. This cause pixels on the edge colums to be floating and thus more noisy.

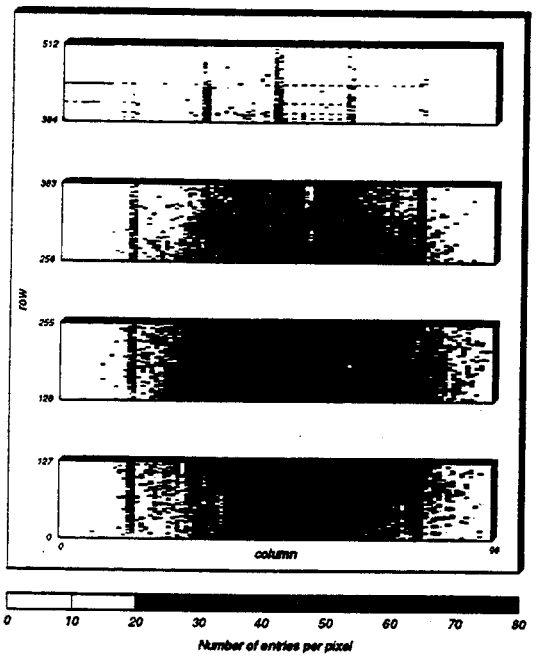

Fig.6: Profile of a Sr^{90} source seen by an Ω3 array. Two millions random triggers were recorded.

spectrometer is $<10^{-10}$ [11]. Taking into account all dead areas and the chips damaged after the array assembly[2], the efficient detector area is 95% for the Ω2 planes and 93% for the Ω3 detectors. Power consumption is 1.1W/array for the Ω2 and 1.8-2.3W/array for the Ω3 system. The consumption per pixel is practically the same in the two detectors. Full efficiency is achieved in both Ω2 and Ω3 detectors for a bias voltage ≥30V [12], [13]. The measured spatial resolution for all the tracks is 23μm in the Ω2 planes [14] and 12μm in Ω3 detectors [12]. The timing resolution of the Ω3 system, measured with both electric stimuli and high energy particle beams is 6ns r.m.s for a single chip and 16ns r.m.s for an array, after tuning the delay adjust registers.

Figure 7 shows the proton beam profile recorded by an Ω3 plane in the NA57 experiment. For more extensive and detailed information on the performance of both the Ω2 and Ω3 systems, the reader can refer to references [6] and [11] - [14].

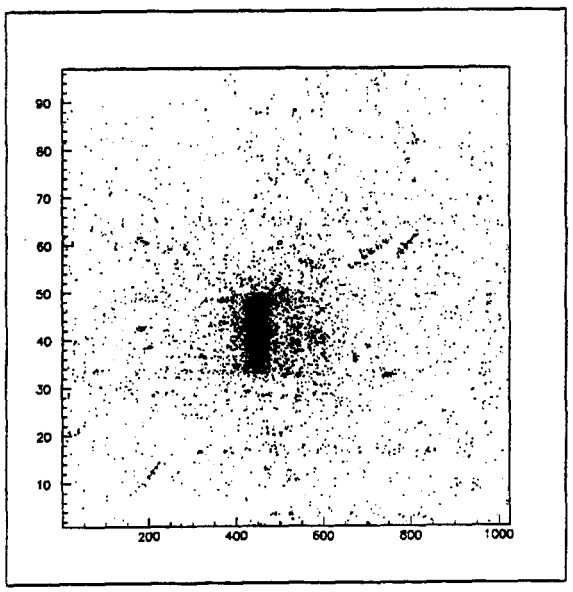

Fig.7: Proton beam profile recorded by an Ω3 plane during the 1997 NA57 run.

Conclusions

Both the Ω2 and the Ω3 pixel system proved to be precise and reliable tracking detectors during four years of operation in WA97 and NA57. They also demonstrated to be capable of handling very high multiplicity events that would have caused any other detector system to fail.

[2] Chips can be damaged while assembling the arrays by Electro Static Discharge or by errors in the mechanical handling

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The Delphi Pixel Detector, running experience and performance

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The DELPHI Silicon Tracker has been optimised to satisfy the requirements of the LEP2 programme. It is made of a barrel part made by microstrip silicon detectors, upgraded from the old Vertex Detector, and the Very Forward Tracker (VFT) in the endcaps, composed on each side by two layers of pixel detectors and two layers of ministrip detectors. The use of pixels is crucial to allow stand alone pattern recognition thanks to the unambiguous three-dimensional determination of the track hit and the high efficiency. This dramatically improves the forward tracking in terms of efficiency and quality in the angular region between 25° and 10° w.r.t. the beam axis.

The Pixel Detector comprises 1.2 million pixels of 330 × 330 μm^2 size with 152 multi chip modules. It was partially installed in 1996, was completed in 1997 and it has collected data for two years. Module efficiency above 96 % and noise level below one part per million have been achieved.

A description of the detector is given and the running experience is reported. Results obtained are presented and the contributions to the forward tracking are shown.

1. Introduction and Motivations

The Delphi Silicon Tracker[1] is designed in order to satisfy the requirements posed by the physics programme at LEP2. The design takes into account the need for good hermeticity, giving emphasis to a good coverage of the tracking in the forward region[2], particularly important at LEP2 because of the following features of the processes studied or searched for:

- four fermion processes, important for both standard and non standard physics are relatively frequent, hence a larger angular coverage in polar angle is required compared to Z^0 physics.
- processes with the largest cross section, such as $e^+e^- \to q\bar{q}\gamma$ or $e^+e^- \to \gamma\gamma$ produce particles predominantly in the forward direction

The tracking below 25° for the Z^0 programme is provided by the forward wire chambers FCA and FCB[3] located far away from the interaction point, at $Z = 155$ cm and $Z = 275$ cm respectively and after more than one radiation length of material. The presence of γs confuses the tracking of forward wire chambers because of the high probability to shower before or between them, therefore creating a region with high density of hits belonging to the shower. In hadronic jets, where all π^0 particles decays into two γs, this causes both a low tracking efficiency and several unassociated neutral clusters in the electromagnetic calorimeters. To improve this situation for LEP2 it has been necessary to build a tracking detector close to the interaction point and able to provide stand alone pattern recognition.

The Silicon Tracker is the upgrade of the Delphi Vertex Detector[4]. The acceptance of the barrel part is extended from 40° to 25° in polar angle and it is made of microstrip silicon detectors, two layers out of three measuring both coordinates. In the barrel region the pattern recognition relies mainly on the tracking detectors, the most important of which is the TPC. In the forward region strip detectors alone are not capable of providing stand alone pattern recognition, due to the enormous amount of spurious combinations of hits and ghosts tracks that would arise.

For this reason pixel[5] detectors are adopted, in order to provide unambiguous three dimensional points with which to build tracks elements with high purity and efficiency. Naively, it could seem an ideal solution to use several layers of pixels detectors, but studies show that a combination of two internal layers of pixel detectors and two external layers of ministrip detectors is an adequate choice, and furthermore reduces substantially the cost of the project. The choice of the cells dimensions is determined by the fact that momentum resolution is limited anyway by Coulomb scattering such that a hit resolution of 100 μm is sufficient.

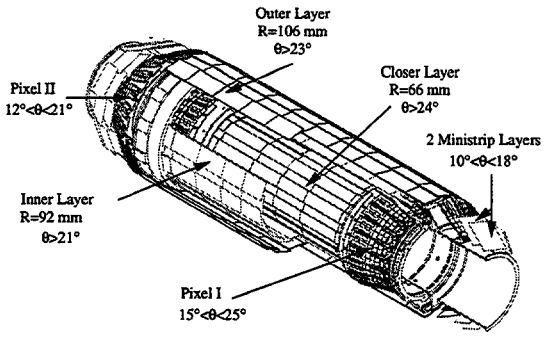

Figure 1. *Layout of the DELPHI Silicon Tracker*

The endcaps of the Silicon Tracker are therefore composed of two layers of pixel detectors, with cells of 330 × 330 μm^2, and two layers of back-to-back ministrips detectors with readout pitch of 200 μm and one intermediate strip. The endcaps cover the angular region 10° – 26° and 154° – 170° and they are called Very Forward Tracker (VFT in the following). The Silicon Tracker is illustrated in figure 1.

The design of the VFT has to satisfy the mechanical requirements on the Silicon Tracker. The space constraints are provided by the inner radius of the Inner Detector and the radius of the beam pipe and the total length of the detector must be limited to 1050 mm, in order to be able to install the structure inside DELPHI. The mechanical design must also be sufficiently rigid to support all components and suffer as little stress as possible from the varying deformations of the different components with changes of temperature, humidity, etc. At the same time, the extra support material must be kept to a minimum, so as to maintain the previous performance for the Rϕ impact parameter resolution in the barrel section. Figure 2 shows diagrammatically a cross section

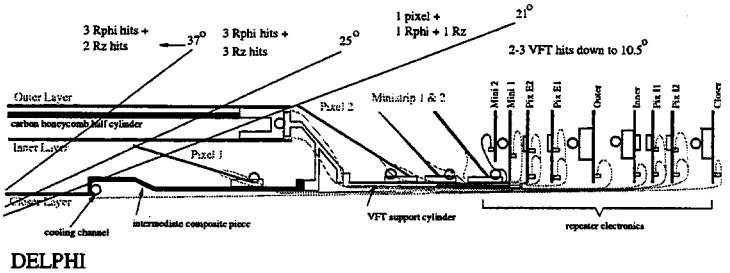

Figure 2. *Cross section of one quadrant of the Silicon Tracker for z>10cm*

of the modules and supports for one quadrant of the detector. It is evident how little is the space available for the internal pixel layer that is accommodated inside the Barrel part and this determines an angle of inclination of only 12° w.r.t. the beam axis.

The mechanical support consists of light aluminium endrings joined by carbon-honeycomb half cylinders. The internal pixel layer is accommodated on a composite piece that connect the endring of the Barrel closer layer with the Barrel endrings. The thermal expansion coefficients between the components are matched to reduce mechanical stress.

An adaptor piece connects the barrel to the forward cylinders. The forward cylinders support the external pixel layer and the two ministrips layers, and also serve to route the kapton cables towards the repeater electronic boards.

The resulting structure maintains the amount of material in the barrel at a similar level to the 1994-95 Vertex Detector, and moves forward material to significantly lower polar angles than previously. A photograph of part of the detector can be seen in figure 3.

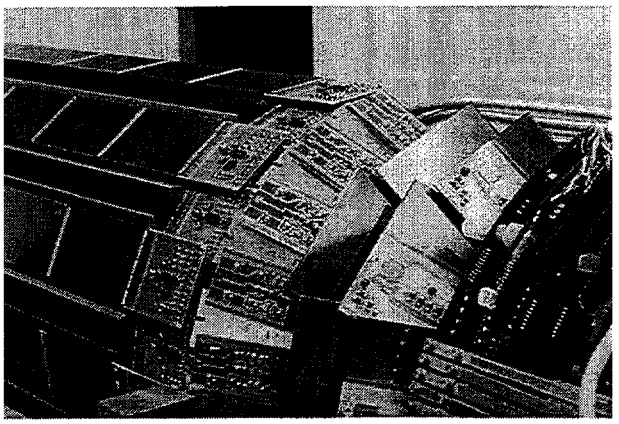

Figure 3. Photograph of part of the detector showing from left to right Rz detectors of the Outer layer with their hybrids, the second pixel layer, two ministrip layers and part of the repeater electronics.

2. Experimental conditions

Before going to describe the Pixel Detector, it is important to define the experimental conditions in which it is working. They are mild compared to those of a hadronic machine.

The time between two crossovers (BCO) at LEP, when running with 4 bunches is 22 μsec, giving the detector no problem to have the data ready to be read out every BCO. The Pixel Detector does not contribute to the trigger and it is read out every second level trigger. The trigger rates are 600 Hz for level one and less than 5 Hz for the second level: readout times are not very stringent.

The radiation level in the detectors is also very mild. It is constituted by off momentum electrons, often showering just in the material before the detector and by syncrotron radiation. The irradiation of the Pixels is estimated to be at the level of < 1 kRad per year.

3. Detector description

3.1. Sensor

A sensor module consist of a pixel silicon detector with p^+ diodes on a n substrate 300 μm thick, with high resistivity of 5-10 kΩcm determining a depletion voltage of 40-60 Volts. It consists of 10 areas each with 24×24 pixel cells and 6 with 18×24 pixel cells, each area corresponding to a readout chip. The pixel cell has a dimension of 330×330 μm^2 but cells in the boundaries between different areas have dimensions doubled in order to avoid dead regions due to readout chips being few hundred μm apart one another. A picture of a sensor is in figure 4 where from the shape it is clear why they are called raquettes. Overall dimensions are length of about 7 cm and width of 2 cm. The Delphi pixels adopt a hybrid solution therefore each sensor is bump bonded to 16 electronic chips. The area available for the bonding on the pixel cell has a diameter of 140 μm.

The digital signal for the electronic chips are routed on the sensor,where a bus is integrated using double metal techniques. A guard ring surround the sensitive area. Supply lines to the chips do not go directly through the integrated bus be-

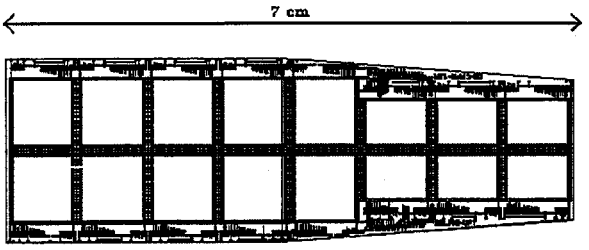

Figure 4. *Pixel sensor*

cause of voltage drop on the resistive lines. A kapton foil is glued instead on top of the chips and distributes the supply lines close to the single chips; then via bonding wire they are connected to the integrated bus and reach the chips.

One raquette has in total 8064 pixel cells. The supplier of the sensor is CSEM[1], the design was done at CPPM[2].

3.2. Readout chip

The readout chip is called SP8[3][6]. It is a VLSI chip in 3 μm technology and provides preamplification, shaping, discrimination and binary readout of cells with signal, using a 2D sparse data scan[7] and each signalled cell is readout in 200 ns. On two cells per chip, a p-well underneath the input pad defines a 30 fF calibration capacitance. The power consumption of the chip is of 40 μW per cell.

The threshold is adjustable between 5 to 20 ke^-, with 1.2 ke^- RMS. From test beam data it has been proven that in the configuration of Delphi Pixel detectors, for a threshold up to 10 ke^-, an efficiency of 99 % is obtained.

The interconnection via the integrated bus is highly demanding in terms of failure rate of the interconnection technique. The connection between the bus lines and the corresponding pad on the chip is achieved by the same bump-bonding technique used for the pixel interconnection. The IBM C4 (Controlled Collapse Chip Connection) bump bonding process[4] was used with 100μm bond diameter on a 140μm diameter bonding area. A $(2.4 \pm 0.2) \times 10^{-4}$ failure rate was achieved, that determines 80% raquette efficiency due to bump bonding.

The SP8 is designed for a milder environment than LHC so it works stably for occupancy < 20% and it has a radiation tolerance of 10 kRad.

3.3. Assembly of a Raquette

The assembly of the raquette module is done in several steps:

- 16 SP8 chips are bump bonded to the detector;
- the ceramic providing the mechanical support of the raquette is aligned and glued;
- the 4 layer flat kapton[5] is glued on top of the SP8 chips;
- long kapton[6], providing the connection to the repeater electronics, is glued;
- wire bonding is done to connect: long kapton to flat kapton lines and then to the bus integrated on the detector; flat kapton to the supply lines on the detector.

The assembly of a pixel raquette is illustrated in figure 5. The complete raquette module determine less than $1\%X_0$ of material budget.

The yield of production at the several steps of the assembly is: 77% after dicing and bump-bonding; 68% for a full functioning of the readout of all 16 SP8 after the connection to the raquette and 85 % for the remaining phase of the assembly, including mounting on crowns and finally on the Silicon Tracker mechanical support. Taking into account also the 82% rate for accepting the sensor before considering the assembly, the total yield rate become of 36%.

[1]CSEM, Rue de la Maladiére 41, CH 2007, Neuchatel, Switzerland
[2]CPPM , Centre de Physique de Particules de Marseille
[3]Designed by College de France, Paris and CPPM; Made by FASELEC 3 μm technology, Phyllips (Taiwan).
[4]Metallisation done by IBM, Corbeil (France); flip-chip by IBM Montpellier (France)
[5]Design of CPPM; Made by TELEPH
[6]same reference of the flat kapton

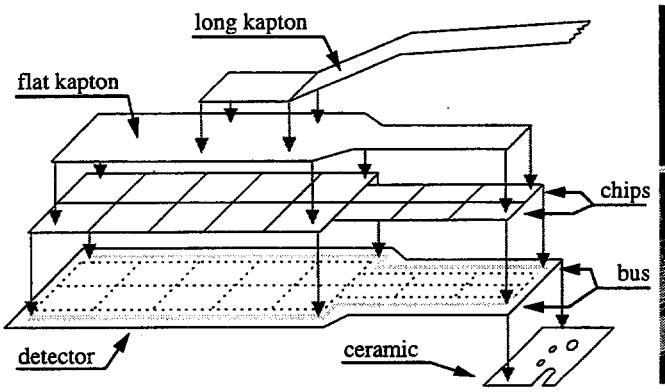

Figure 5. *Assembly of a pixel raquette*

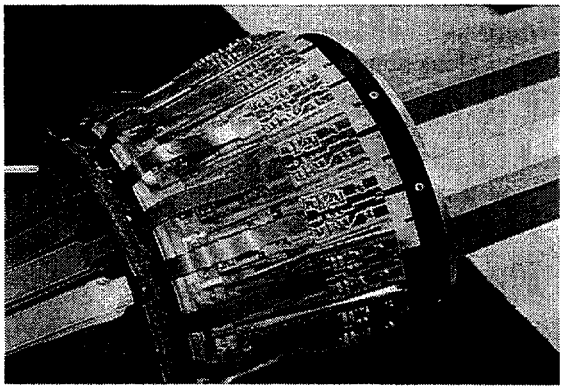

Figure 6. *Photograph of a assembled inner layer pixel crown.*

3.4. Crown

The pixels raquettes are mounted onto semicircular aluminium supports, with inclinations with respect to the z axis of 12° and 32° for the pixel and are arranged in groups of 19 forming a pixel crown. The raquettes are connected to the repeater boards with the long kapton cables, with two repeater boards per crown. A photograph of a pixel crown is shown in figure 6. There are 8 crowns, for a total of 152 raquettes and 1.2 millions pixels for a sensitive area of 0.2 m^2.

Overlap between adjacent raquettes is provided in order to allow internal alignment: for the inner and outer pixel layers the overlap corresponds to 37% and 12%.

3.5. Readout system

The readout system[7] consists of a crate processor housed in a fastbus crate controlling 4 fastbus modules (PIxel Read-Out Modules PIROM) and reading them sequentially. Each PIROM contains 4 PIxel Read-Out Unit (PIROU) based on a micro-controller Motorola 68332, connected each one to one repeater board, and all PIROU are read in parallel. Each PIROU controls a group of 10 or 9 raquettes connected to the repeater, addressing and reading sequentially each chip of each raquettes. The readout scheme allows the skipping of malfunctioning/not responding chips. A mask of noisy pixels can be loaded on the PIROU in order to suppress them: this is particularly important in order to keep the size of the pixel data low avoiding unnecessary information.

3.6. Slow Control system

Stable and safe operation is a critical issue for running the Pixel Detector. There is an automated response to changes in the data taking conditions or possible misbehaviours of the detector, running within the framework of the general DELPHI slow controls system.

The slow control frontend-computer for the Pixel[9] is based on a 68340 processor running OS9 and the main components are a commercially available SY527 CAEN and a home made DAC-system.

The CAEN[7] controller supervises power supplies and depletion voltages for a total of 88 channels, distributed at the level of repeater or crown. The threshold settings is done at the level of single raquettes in order to optimise the working point of each one in terms of efficiency and noise per-

[7] Costruzioni Apparecchiature Elettroniche Nucleari S.p.A., Via Vetraia, 11, I-55049 Viareggi, Italy

formance. It is controlled by the DAC system

A procedure was developed to detect and react to an anomalous number of hit pixels, associated to either a high background or to a misbehaving chip. It is necessary to protect the detector against accidental very high occupancies because the power consumption of a cell connected to a hit pixel increases by a factor of about 10. If the required power exceeds the supply characteristics the detector may then trip off, leading to a jump in temperature of around 12°C, affecting badly the detector stability. A typical situation where this can arise is during the LEP injection, when the occupancy can be up to more than 2 orders of magnitude greater than nominal. When the occupancies are abnormally high the crate processor supervising the data acquisition notifies the slow control system, which raises the thresholds [9]. In addition, for the special period of LEP injection when the backgrounds are expected to be high, the discriminator thresholds are always automatically raised.

4. Performance

4.1. Noise level

The level of systematically noisy pixels is around 0.3%. Most of the noisy pixels are removed by masking in the crate processor, and the remaining ones, defined as those which respond to more than 1% of triggers, are flagged and removed off-line.

After the removal of noisy pixels, the hits which remain originate from particles traversing the detector and from random noise. The number of pixel hits is shown in figure 7 for three classes of events. Hadronic events, where some tracks pass through the forward region, have a mean number of pixel hits of about 4.5. Background events, which are triggered events with no tracks pointing to the primary vertex, include beam gas interactions at low angle and off-momentum electrons than might have showered before the Pixel, and result in a tail extending to very large numbers of hits. Such events become more prevalent at higher energies.

A class of events was also selected with just two charged tracks reconstructed in the barrel. These events should produce no physics background in the forward region, and the mean number of pixel hits places an upper estimate on the random noise of 0.5 ppm.

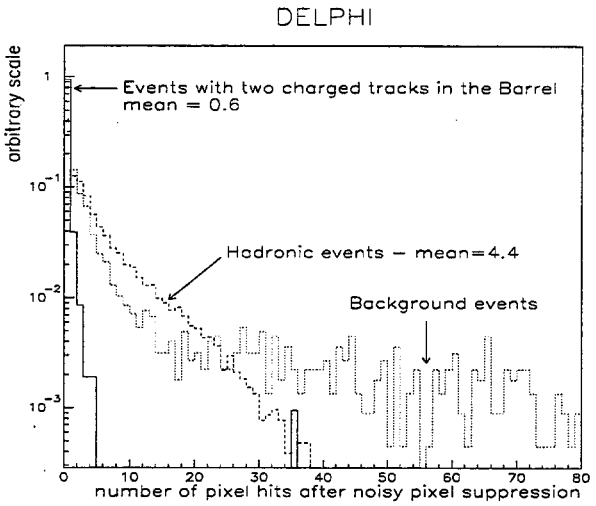

Figure 7. *Mean number of pixels per event for hadronic events, background events, and events with two charged tracks only in the barrel. The data are taken from the 1997 Z^o running period. The normalisation is arbitrary.*

4.2. Alignment

The alignment of the full Silicon Tracker consists of a survey stage and an alignment using tracks.

The pixel detectors are surveyed in two steps. After the chips are bump-bonded and the ceramic support is glued to the detector, the two-dimensional position of the external detector corners and the ceramic are determined with a microscope with respect to pads close to the detector corners.

These pads have a well known position on the detector mask and define the position of the pixel

array. They are chosen as a reference as they remain visible during the assembly. The kapton cables are then attached and the tested module mounted on the support. Its position, given by the location of the two corners plus the measurement of the module's plane, is related to that of three spheres mounted on the support. After all modules are mounted, the VFT crowns are joined to the barrel support and the positions of the spheres with respect to the barrel are measured.

Being the survey made before the installation inside DELPHI, the survey gives no information on the relative position of the two half-shells. Also the geometry of either half-shell after installation might slightly differ from the results of the survey, due to possible deformations of the mechanical structure. The survey is therefore the starting point for the alignment done using tracks.

The VFT alignment procedure uses track elements already reconstructed with the use of the other tracking detectors. The procedure optimises the VFT module positions by minimising the χ^2 of tracks refitted over all track elements. The weight of a track in the fit depends on the polar angle and the combination of tracking detectors contributing to the track. In addition, the intrinsic VFT resolution and the constraints from overlapping modules are exploited. The global parameters at the level of each quadrant are determined first, then the individual plaquette parameters are fitted, allowing 6 degrees of freedom per plaquette. The overlap between the first pixel layer and the Barrel Inner layer at $20° < \theta < 25°$ provides a good link between the Barrel and the VFT global alignment.

4.3. Efficiency

The efficiency of the pixels was studied using tracks which pass through a region where neighbouring plaquettes overlap and have at least one hit in a silicon layer other than the one being studied. If a track registers a hit in one plaquette, a second hit is searched for around a 3σ window in the neighbouring plaquette. Figure 8a shows the average efficiency measured in each pixel crown using this technique. The average efficiency excluding bad plaquettes was 96.6%.

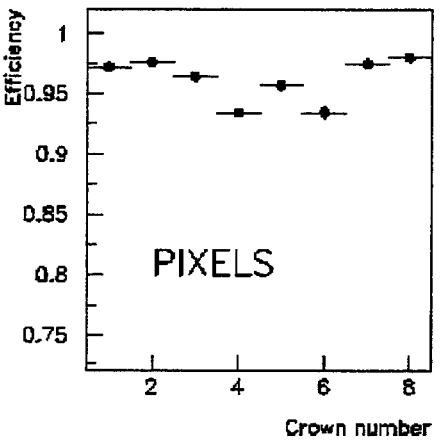

Figure 8. *Efficiency for the pixel crowns as measured inthe 1997 data using tracks (see text). The average quoted efficiencies do not take into account dead modules.*

4.4. Resolution

For the pixels, the expected resolution depends on the cluster size, which is a function of the track incidence angle. Tracks from the primary vertex traverse the first and second pixel layer at incidence angles ψ in the polar direction of 57.5° and 40.5° respectively. The incidence angle in the $R\phi$ direction is close to 90°. The majority of produced clusters are either single hits or double pixel hits split in the polar direction. Neglecting charge diffusion effects, the angular dependence of the single pixel hit rate is given to first order by the following equation:

$$N = (1-\frac{d}{\Delta}); \qquad d = w \times \tan\psi - \frac{t}{c} \times w \times \sin\psi (1)$$

where w is the thickness of the depletion layer, Δ is the pixel pitch, c is the charge deposited by a minimum ionising particle and the parameter t is given by the detector threshold (about $10ke^-$ is used). Knowing this rate, a simple geometrical consideration of ionisation charge sharing in the pixel sensitive volume leads to the following

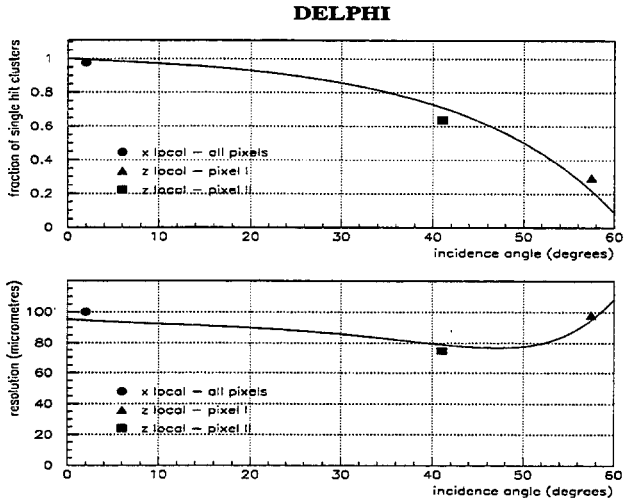

Figure 9. *Resolution expected in the pixels as a function of track incidence angle (solid line) shown together with the values measured in the data.*

expression for the expected detector resolution:

$$\sigma^2(\psi) = \frac{1}{12}\frac{(d^3 + (\Delta - d)^3)}{\Delta} + (\frac{\kappa}{c} \times w \times \sin\psi)^2 (2)$$

Here κ is a parameter describing the effect of charge fluctuations (about 5ke$^-$ is used), and the other symbols are the same as in equation 1.

The expected distributions are displayed in figure 9 as a function of ψ. The resolutions in the data are measured in the detector plane for the z_local (polar) direction and the x_local ($R\phi$) direction. The values extracted are overlaid on the prediction. For the x_local points the incidence angle is the same for the pixel I and pixel II layers, and these points are shown together. The measured points are seen to be very close to those predicted by the simple model.

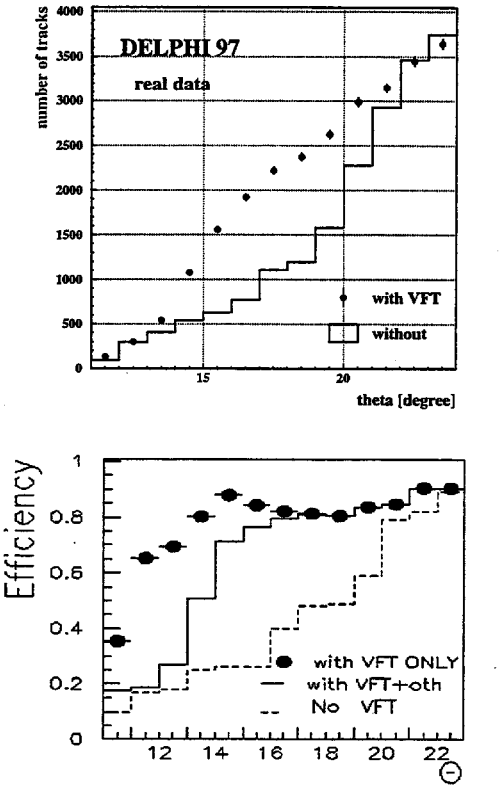

Figure 10. *Improvement on the forward tracking thanks to the Pixel Detector in the VFT*

5. Improvement in Forward Tracking and Hermeticity

Improvements of the forward tracking using the VFT data have been studied both at Montecarlo level, using the full reconstruction software of Delphi, and on real data. The performance of the tracking both excluding and including the VFT data has been been compared.

In the upper part of figure 10 is the number of tracks versus polar angle for real data collected in 1997, when including or not the VFT in the tracking. To measure an absolute tracking efficiency on real data is difficult since there is no redundancy in the forward tracking to do so. Therefore in the lower part of figure 10 is the tracking efficiency as measured on MC, with and without VFT.

Comparisons on data/MC of the ratio of number of tracks obtained with and without VFT give a good agreement giving confidence on values found by the MC studies.

When quoting *with VFT* is meant that the VFT is contributing to form a track together with another tracking detector (mainly FCA and FCB).

It was mentioned in the beginning of the paper that VFT provides standalone pattern recognition, and in certain cases a good VFT track might not find a clear association to the other tracking detectors. These tracks, called VFT only tracks, reach a high purity, greater than 95% when including hits from 3 layers and therefore they improve substancially the tracking hermeticity down to about 10°. In figure 10 is shown the tracking efficiency obtained when this category is added. The VFT only tracks have a poor momentum resolution but the direction of the track at the VFT is measured with 1-2 mrad precision. The use of the VFT only tracks is exemplified in picture 11 where a real event having two high energy deposit in the electromagnetic calorimeters but no tracks associated to them is shown. Including VFT only tracks, two tracks are visible, allowing to determine that the event is a Bhabha in the forward direction.

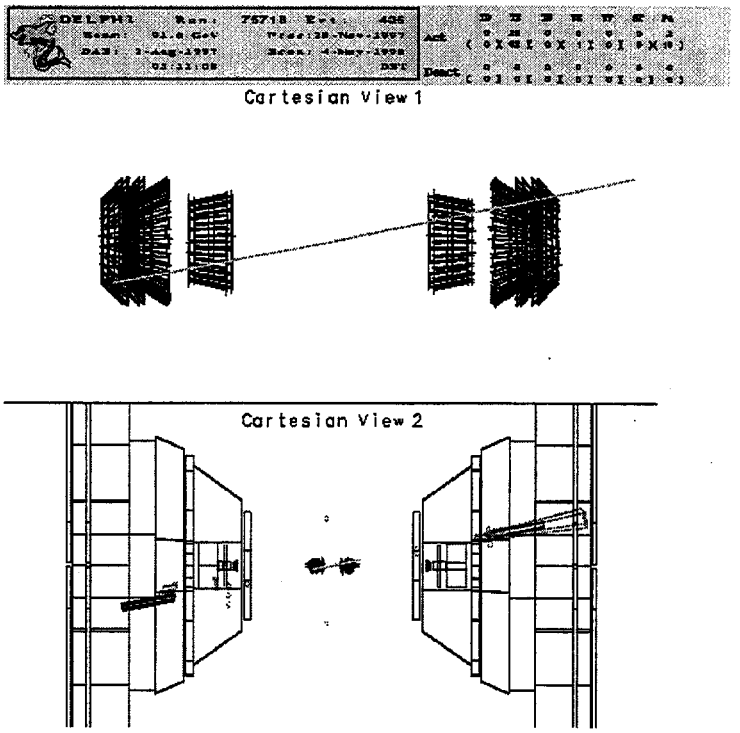

Figure 11. *Bhabha event with tracking provided by the VFT*

6. Conclusions

The Delphi Pixel Detector was commissioned on 1996 and then completed on 1997. Stable running performance have been obtained and the design performance has been achieved: random noise level of 0.5 ppm and single plane efficiency of 96% with a hit resolution of 80-100 μm.

This allows Delphi Silicon Tracker to satisfy the request imposed by the LEP2 programme. The VFT has been fully integrated in the tracking of Delphi and this has dramatically improved the tracking efficiency in the forward region.

Acknowledgements

This paper is presenting the results achieved thanks to the common effort of the entire Delphi Pixel group. I want to thank all my colleagues for the brilliant work done and for having supported me for this presentation.

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The ATLAS Pixel Detector

Guido Gagliardi, University and INFN Genova

on behalf

ATLAS Pixel Collaboration [1]

Albany, Berkeley, Bonn, Dortmund, Irvine, Genova, Marseille, Milano, Nikhef, New Mexico, Oklahoma, Prague, Santa Cruz, Siegen, Toronto, Udine, Wisconsin, Wuppertal

Abstract

The ATLAS Pixel Detector is presented in the context of ATLAS detector at LHC: the role of Pixel Detector in the tracking system is shown. The layout of the Pixel Detector is described. The pixel detector has a modular design, made by three barrels and 10 disks which are in turn made by modules: the detector uses the same modules for the barrel and disk region.The Read-Out architecture of a module is presented in particular detail. The electronic in a module consists of 16 Front-End (FE) chip which build the hits and a Module Control Chip (MCC) which builds the event and re-routes the fast and slow commands from the control room to the FE's. The expected performance of the Pixel Detector in the tracking system is reported. Results on the required bandwidth and buffer size are also reported.

1. Introduction.

The ATLAS collaboration is developing a Pixel Detector as a vertex detector for the Inner Detector tracking system[2][3]. The role of tracking in the experiments which will be positioned in the Large Hadron Collider (LHC) has increased with the time, subsequently to the effort done in the understanding the behaviour of the tracking system in the LHC high luminosity environment.

One of the features one requires from the tracking system in the LHC experiments is the ability to identify hadronic jets containing a b quark (*b-tagging*). Many of the interesting physics channels at LHC benefit from a good b-tagging: among them there is the $H \rightarrow b\bar{b}$ channel, which could increase the signal of a low mass Higgs ($m_H < 130$ GeV); the $H \rightarrow hh \rightarrow b\bar{b}b\bar{b}$ channel (if the heavy MSSM Higgs can couple to two light Higgs); and virtually every channel that involves the t quark, as, for example, the t quark decaying into a charged Higgs and a b quark. To obtain a good b-tagging is mandatory to have a vertex detector as close as possible to the interaction point.

The tracking detectors near the interaction point in LHC must cope with high instantaneous and integrated particles rates. The LHC high luminosity (the project luminosity is 10^{34} cm^{-2} s^{-1}) is obtained by circulating 2835 proton bunches with small interaction cross section and up to 10^{11} protons per bunch. The time between two Bunch Crossing Over (BCO) is 25 ns. The number of collision for bunch crossing depends on the pp cross section: the expected value is ~25 pp interaction per BCO.

The high instantaneous rate implies fast detectors and fast Front-End (FE) and read-out electronics, with some pipeline memory close to the detector to store data while the trigger decision is pending. A good granularity is also required since the expected number of charged particles per interaction is ~7 per pseudorapidity[4] unit: in the $-2.5 < \eta < 2.5$ region there are about 10^3 charged particles per BCO. The high integrated rate implies that all devices and material should keep operating after a very high radiation dose (up to 30 MRad).

It is natural in this context to adopt a pixel detector as a solution for the vertex detector in ATLAS. Pixel detectors are fast; hybrid pixel detectors which are composed of a sensor bump-bonded to a front-end chip can use the front-end chip area to perform complicate task and act like a local memory; pixel detectors provide both granularity and high

signal-to-noise ratio to cope with the high luminosity LHC environment.

2. ATLAS Pixel Detector Layout

The ATLAS Pixel Detector is shown in Figure 1. The layout covers the eta region $|\eta| < 2.5$ and provide at least three space points.

The Pixel Detector is made of three barrel in the

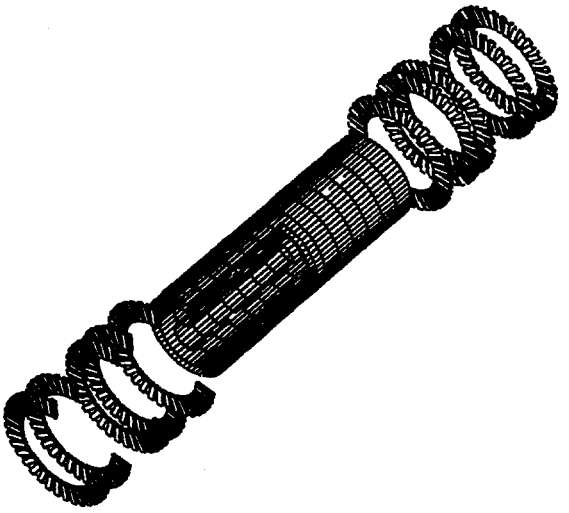

Figure 1: ATLAS Pixel Detector Layout

central region and 5 wheel in each of the forward regions. This geometry guarantees always a high incidence angle between the particles and the silicon sensors.

The barrel pixel tracker is made of pixel modules arranged in three cylindrical layers - the parameters are given in Table 2-1. The inner layer is called "B-Layer" since is the nearest to the interaction region and allows the precise measurement of impact parameter of the particles and of the secondary vertexes.

The barrel modules are arranged end-to-end on long 'ladders' which lie parallel to the z-axis - 13 modules per ladder. Overlap of the active area in the z-direction is achieved by having alternate modules shifted 0.03 cm above and 0.03 cm below the mean radial position, with the central module being located at the larger radius.

Each end-cap pixel tracker is made of the same modules as those in the barrel, with 250 μm pixel sensors used throughout, arranged in rings of 36, which are mounted on either side of disks which provide support and cooling.

Modules which are adjacent in ϕ are mounted on alternate sides of the support disk. The two rings are spaced in z by 0.7 cm and are identical except for a 5° rotation in ϕ in order to insure hermeticity. The parameters of the 5 disks are given in Table 2-2.

Table 2-1 Parameters of barrel pixel layers.

Layer	R[a] (cm)	Active half-length (cm)	Number of modules in z	Number of ladders in R-ϕ	Tilt angle (degrees)
B-layer	4.3	38.9	13	18	- 15.0
Layer 1	10.1	38.9	13	42	- 11.4
Layer 2	13.2	38.9	13	56	- 11.4

a. The radius is defined as the position of the centre of the sensitive silicon for the central module.

Table 2-2 Parameters of pixel end-cap disks.

Wheel number	z positions (cm)	Active R_{min} (cm)	Active R_{max} (cm)
1	49.52	12.63	18.67
2	61.18	12.63	18.67
3	66.95	12.63	18.67
4	84.12	12.63	18.67
5	92.61	12.63	18.67

The grand total of modules in the ATLAS Pixel Detector is 2228. In Figure 2 is shown the material in

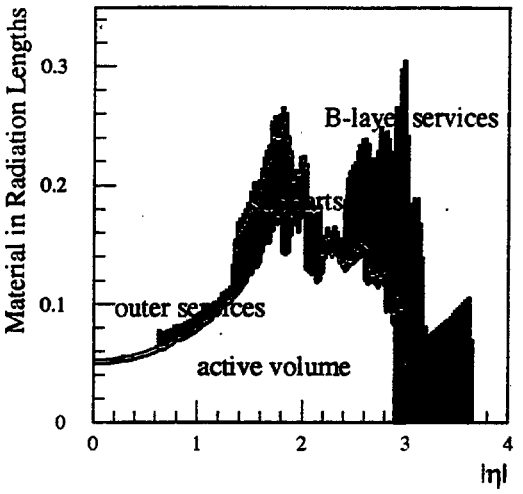

Figure 2: Material in radiation lengths in the Pixel system as a function of eta. The *active volume* includes sensor, hybrids, read-out electronics and optical links; the *supports* include mechanical supports.

radiation length of the ATLAS Pixel Detector as a function of the pseudorapidity of incident particles. The barrel supports are at $\eta = 2$. It must be pointed out that the B-Layer supports, also shown in the Figure 2, contribute with a big amount of material to the total material budget at large η, since they are routed along the beam pipe. This choice allows periodical replacement of the B-Layer, which is supposed to survive a few years at the nominal LHC luminosity.

3. Pixel Detector Modules

Modules are the basic building blocks of the ATLAS Pixel Detector. A module consists of the silicon sensor tile, the read-out electronics, the local signal interconnections and power distribution busses, and passive components such as temperature sensors, resistors and capacitors.

The sensor tile is made of 61440 pixels. The pixel shape is rectangular, 50(rϕ) x 300(z,r) mm. The asymmetric shape is chosen to achieve best performance in the transverse plane[1]. The ATLAS Pixel Detector choice is to do not have any information on the energy released in the pixels (binary read-out): the small pitch in the rϕ direction together with the tilt angle, oriented to minimize the charge spreading due to the Lorentz force[2], is thus providing the optimal spatial resolution.

3.1. The read-out electronics

The read-out electronics has the task to build the hits (stream of data representing the passage of the particle through the sensor), to sparsify them and to reduce the amount of data[5].

The ATLAS Trigger System is structured in three levels: the first level (LV1 trigger) has a input bandwidth of 40 MHz and a decision time (latency) of 2.5 μs. Because of the high input rate, data are supposed to stay inside the detectors during the LV1 latency time: only data belonging to a LV1 accepted event are transferred to the next trigger levels. Another task for the read-out electronics is to store data during the LV1 latency time and to retrieve and send out data with a time resolution of 25 ns.

The read-out electronics of a module is structured in a two-level architecture. The first level is made of

[1] In the ATLAS coordinates the z axis go along the beam pipe and the transverse plane is perpendicular to the z axis.

[2] The ATLAS Pixel Detector is posed in a 2 T solenoidal magnetic field.

16 FE's, bump-bonded to the sensor tile. The FE's build, sparsify and store the hits during the LV1 latency time. The second level is made of a Module Control Chip (MCC). The MCC builds the event collecting together data from the 16 FE's and redirects the control signals and the clock to the FE's.

The module read-out architecture is shown in

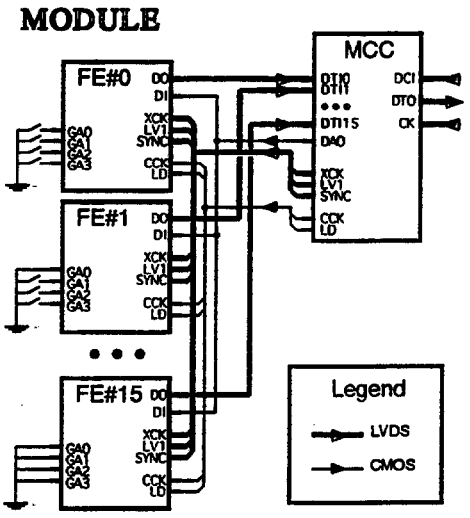

Figure 3: Module read-out architecture

Figure 3. It is a data push architecture: the FE hits are transmitted as soon as they are ready. All data link between the FE's and the MCC, and between the MCC and the Read-Out Buffer (ROB, the external buffer electronics) are serial. The interconnections have been kept very simple, and all connections which are active during data-taking use low-voltage differential signalling (LVDS) standards to reduce EMI and balance current flows. Other signals use full-swing single-ended CMOS to reduce the pin count. The LVDS data links allow a bandwidth of 40 Mb/s.

The FE's and the MCC are connected with a point-to-point topology that ensures fault tolerance and parallel data read-out from the FE's: this allows a better bandwidth usage and smaller buffers in the FE chip. Each FE chip is identify by geographical addressing.

Each FE has a LVDS data line (DO) connected to the MCC; all FE's shares a LVDS line for the clock (CK), the LV1 accepted signal (LV1) and the fast reset (SYNC). The MCC has 16 LVDS data input lines, one for each FE, and three LVDS connection to the external: the input command line (DCI), the output data line (DTO) and the clock.

3.2. The FE's

There are at the moment two architecture for the FE chips: FE-A, which is developed by Bonn and Marseille groups, and FE-B, which is developed by LBNL[5][6].

Both FE chip are organized in 24 column (mirrored in pairs), each column in turn is made of 160 read-out pixel cells, one for sensor pixel (Figure 4).

The pixel cells are composed by a preamplifier that amplifies the charge released by the particles in the sensor, and a discriminator that identifies the over-threshold signals. Each pixel cell sends as soon as possible the information of which cell is hit and when (timestamp)[3] to the End of Column (EoC) logic. this information is called "hit".

The EoC logic stores the hits into buffers (EoC buffers) during the LV1 latency time. At the LV1 accepted signal the EoC logic retrieves in the buffers only the hits with the correct timestamp and serializes them out to the MCC.

As optional information the FE's provide, for each hit, a Time Over Threshold value which can be used as a coarse measure of the released energy in the pixel.

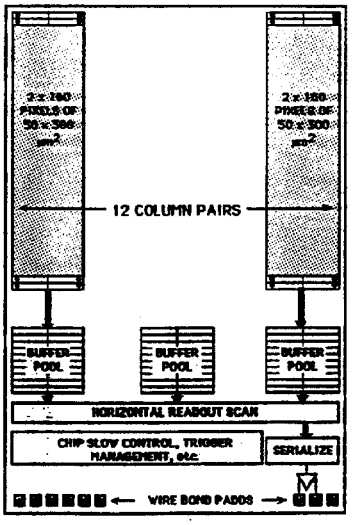

Figure 4: FE chip schematic.

[3] The timestamp is added to the cell number information only in the FE-B scheme, while in the FE-A it is built by the EoC logic.

3.3. The MCC

A floorplan of the MCC[5][7] is shown in Figure 5.

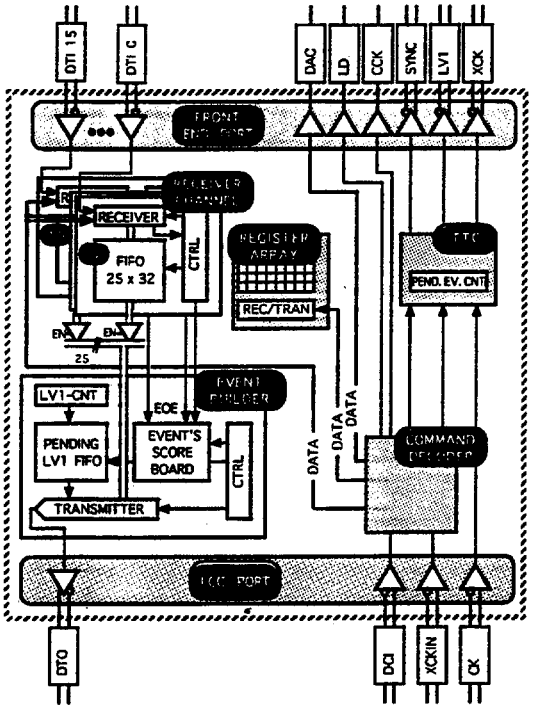

Figure 5: MCC schematic.

The MCC basic blocks are 16 Receivers and an Event Builder. The 16 Receivers collect hits from the FE's and store them until all the FE's have sent the hits belonging to a LV1 accepted event. When all hits are collected, the Event Builder scans the Receivers and serializes out the event.

There are in the read-out electronics two buffer levels: in the FE's the buffers store the hits until the LV1 accepted signal; in the MCC the buffers store the hit until all the FE's have sent the hits belonging to a LV1 accepted event. Local fluctuation of occupancy in one FE thus has a minor impact on the buffer occupancy in the other FE's.

Other tasks of the MCC are the FE's control, the handling of the LV1 accepted signal and the redistribution of the clock.

4. Pixel Detector simulated performance

A complete GEANT simulation of the ATLAS Pixel Detector including all services and mechanical supports has been done. LHC events has been simulated as well.

The results of the simulation has been used to adequately dimensioning the buffer sizes in both the FE's and the MCC, and the maximum available bandwidth between the FE's and the MCC and between the MCC and the ROB's.

In Figure 6 is reported the average double column occupancy per event in both the B-Layer and the Layer 1. The occupancy in the B-Layer is a factor 5

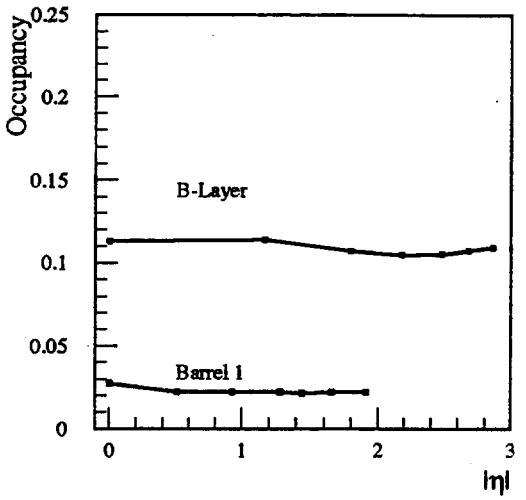

Figure 6: B-Layer and Layer 1 double column occupancy as function of eta

greater than the Layer 1. It is clear that the B-Layer is more demanding for the read-out electronics than the other components of the Pixel Detector. The single pixel occupancy per event is very small as expected for the high granularity pixel detector.

In Figure 7 is shown the data rate from the FE's to the MCC as function of the pseudorapidity of the module. The dotted curves correspond to the presence of the ToT information; continuous curves are for the binary read-out. The average data rate is of the order of few Mb/s, which fit nicely in the 40 Mb/s maximum available bandwidth. The value are similar for the B-Layer and the Layer 1 because for each LV1 accepted each FE's send the hits and a end-of-event word, which is present even in empty event. This end-of-event constitutes the main component of data traffic between the FE's and the MCC.

In Figure 8 is reported the average data rate from MCC to ROB as function of eta. For the Layer 1 the average value is of the order of 10 Mb/s, which is still acceptable for the 40 Mb/s of maximum available

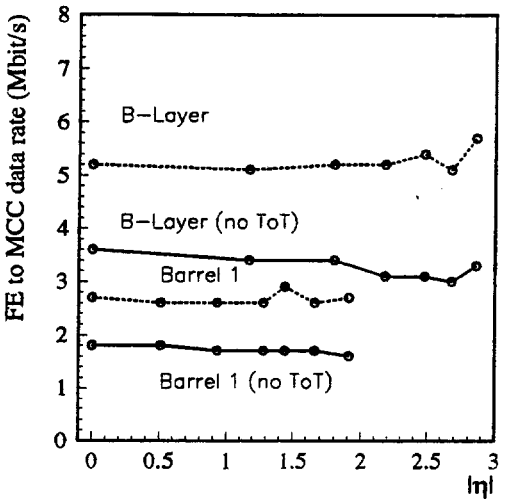

Figure 7: FE to MCC data rate as function of eta.

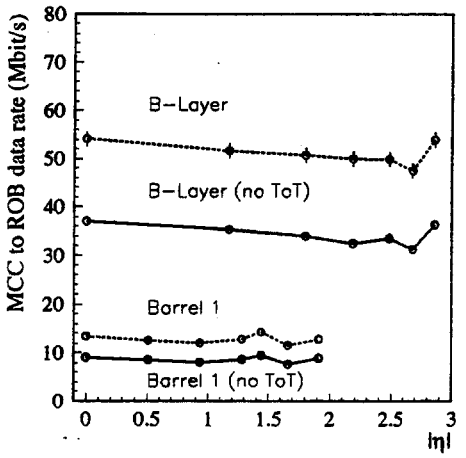

Figure 8: MCC to ROB data rate as function of eta

bandwidth; for the B-Layer it is clear that the maximum available bandwidth should be doubled to cope the 40-60 Mb/s average data rate[4].

A detailed study[3] has been performed to understand the MCC and FE buffer occupancy and the inefficiency induced by the read-out architecture in the Pixel Detector. The results show that the B-Layer is very demanding in the buffer size: the inefficiency induced by the MCC buffer size is less than 1% with 32 buffer per Receiver, but the inefficiency induced by the FE buffers is of the order of 3-5% only with a sizeable amount of buffer, 25-30. This is because the FE's chip store for 2.5 μs (the LV1 latency time) all the hits that occurs in a column pair, while the MCC Receivers store only LV1 accepted events for the time needed to complete the extraction of data to the ROB's. The Layer 1 is less demanding and, with the same buffer size than the B-Layer, virtually deadtimeless.

In Figure 9 is reported the resolution in the transverse plane for the B-Layer.

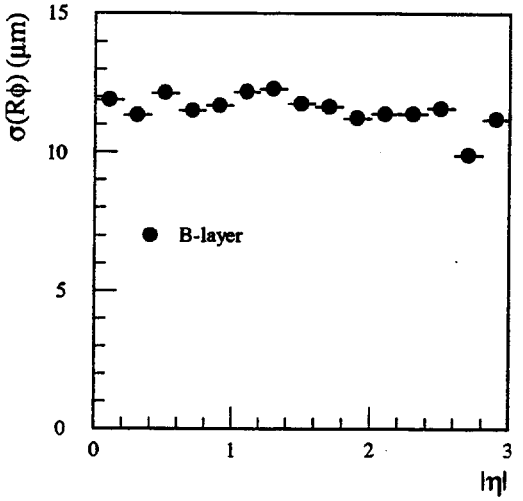

Figure 9: rφ resolution in the B-Layer as function of the pseudorapidity.

The presence of the B-Layer also at high luminosity is crucial for the b-tagging. In Figure 10 it is shown the transverse impact parameter as a function of the p_T of the particles for two different configuration of the ATLAS Inner Detector, one with the B-Layer and the other one without. The effect of the B-Layer is to increase the asymptotic resolution as well to increase the resolution at low p_T. With the B-Layer the light quark rejection at 50% of b-tagging efficiency is ~120[3].

[4] This is foreseen in the Pixel Detector by doubling the number of optical link in the B-Layer, or by doubling the available bandwidth.

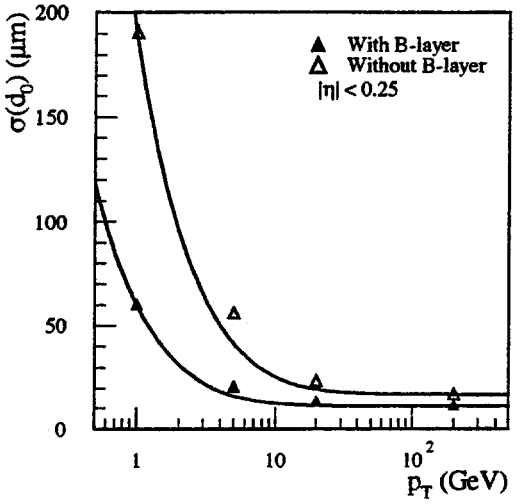

Figure 10: Impact parameter resolution as function of the pT of the particles. The two curves correspond to a Pixel Detector with or without the B-Layer.

5. The Demonstrator programme

In order to demonstrate the feasibility of the ATLAS Pixel Detector a demonstrator programme has started. Pixel Detectors are currently used in several particle physics experiments (SLD, WA97, DELPHI, NA57), but in a much less demanding environment than the one foreseen at LHC.

The main steps of the demonstrator programme are: a single chip bump-bonded to a ~0.6 cm^2 sensor (single chip module); a set of 16 FE's bonded to a sensor tile and connected to a MCC, with the MCC not integrated on the module (16-chip module); and finally the ATLAS module with the MCC integrated on the module.

The main differences between the demonstrator

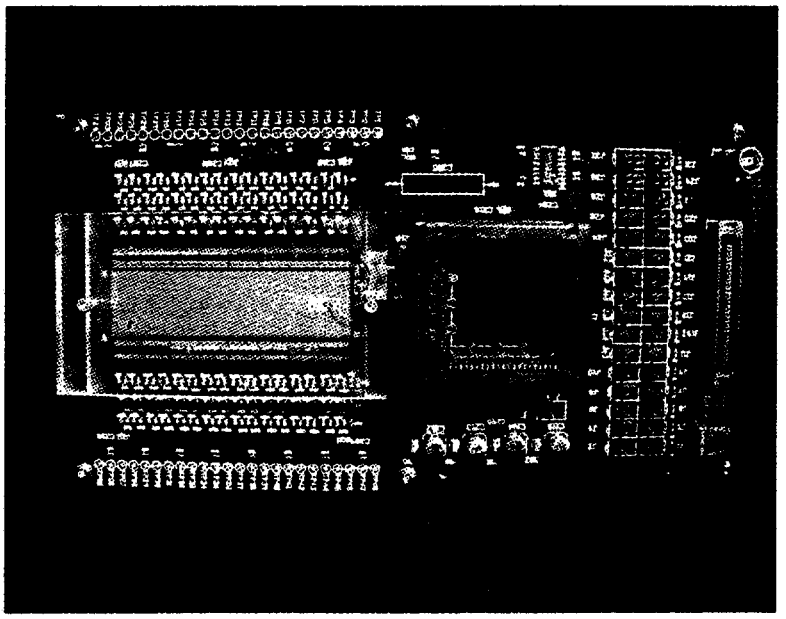

Figure 11: 16-chip module prototype.

and the final design are: all the electronics are designed in rad-soft technology; the number of FE EoC buffers is limited (i.e. sufficient for the outer layers, but not for the B-Layer at nominal luminosity); the pixel cell size is 50 μm x 400 μm; the data transmission from the MCC to the ROB uses copper lines, instead of optical links.

The demonstrator programme has so far produced two different FE chips (FE-A and FE-B), both of them functional to LHC environment; a MCC, that has to

be tested on the test beam on August 1998; and a module prototype (16 FE-A and 16 FE-I bump-bonded to the sensor). In Figure 11 a prototype of a 16-chip module is shown.

6. Conclusion

The ATLAS Pixel Detector is the nearest detector to the interaction point in the ATLAS spectrometer. The main reason to adopt pixel detectors as vertex detector in ATLAS is that only pixel detectors can survive at the radiation damage so close to the beam in the LHC environment; furthermore, pixel detector high granularity guarantees a very low occupancy even at few centimetre from the interaction point, of the order of 10^{-4} hits per pixel per event.

The Pixel Detector is made of modules, that are read-out individually. The module read-out architecture is structured in two levels: the first level (FE chips) builds the hits, the second level (MCC) builds the events and transmits them.

A detailed simulation showed that the data rates are compatible with the maximum available bandwidth. The derandomizing buffer size required to have a less than 1% inefficiency in the MCC is easily obtained, while an effort has to be done to reduce the inefficiency in the FE chips.

However, it is clear that dimensioning the system for reasonable performances in the B-Layer leads to over-dimensioning it for the outer layer of the ATLAS Pixel Detector.

Prototypes of the read-out electronics and sensor tiles have been built and operated in test-beam. These prototypes contains a full LHC logic.

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CMS PIXEL

D. Bortoletto

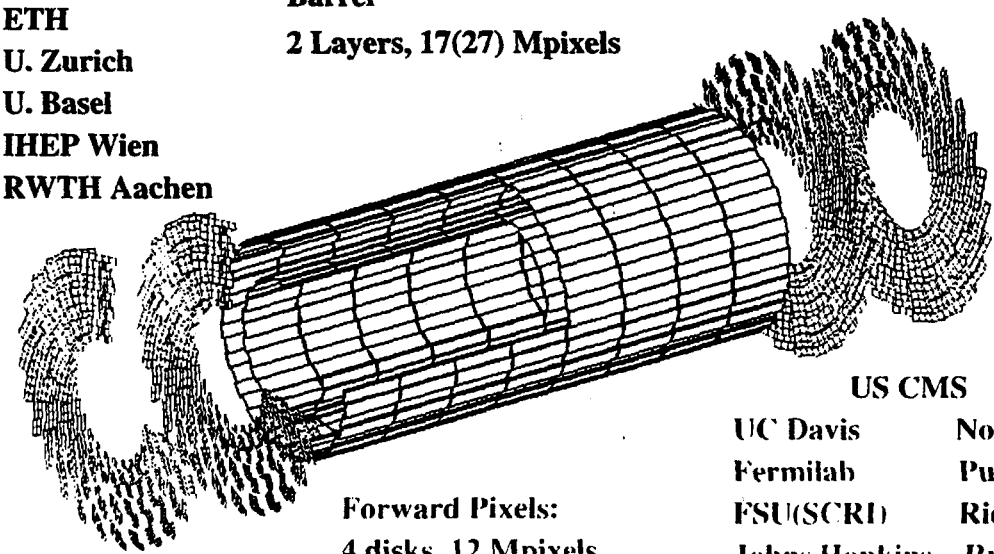
Pixel98 FNAL May 7

- Physics requirements and layout
- Modules, Mechanics and cooling
- Design concerns: material, services, access
- Sensors R&D, specifications and prototyping
- Readout electronics
- Bump bonding
- Summary

Collaboration

PSI (Horisberger)
ETH
U. Zurich
U. Basel
IHEP Wien
RWTH Aachen

Barrel
2 Layers, 17(27) Mpixels

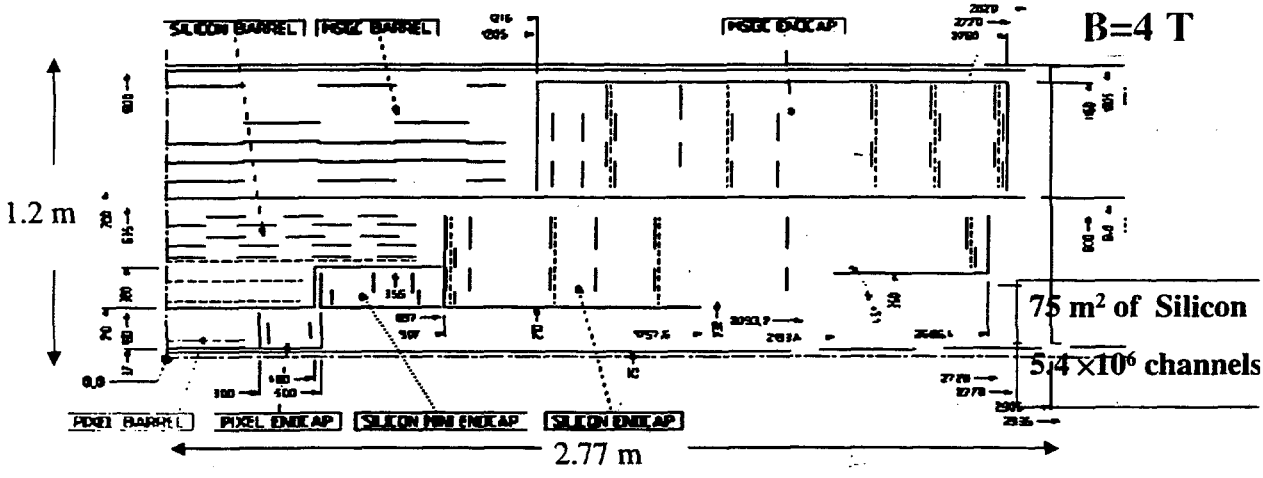


Forward Pixels:
4 disks, 12 Mpixels
$1.5<\eta<2.5$

US CMS

UC Davis	Northwestern
Fermilab	Purdue
FSU(SCRI)	Rice
Johns Hopkins	Rutgers
Los Alamos	Texas Tech
Mississippi	

CMS Tracking

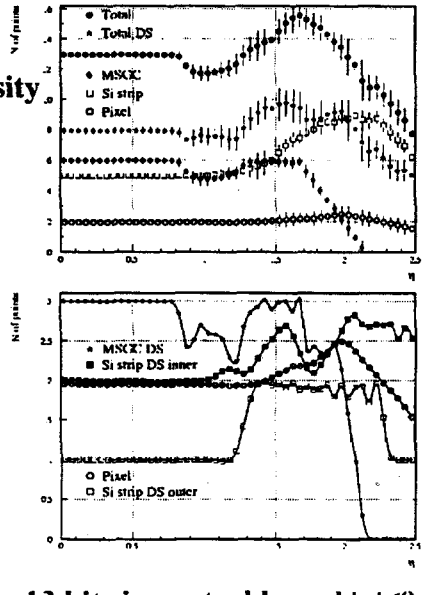


Phase I (Low Luminosity) : First Pixel layer at 4.cm; Silicon: Omit L4 and 2 end-cap disks; MSGC: Omit L4 and 2 end-cap disks

Phase II (High Luminosity): First Pixel layer at 7cm. Instrument missing silicon and MSGC layers.

Layout Optimization

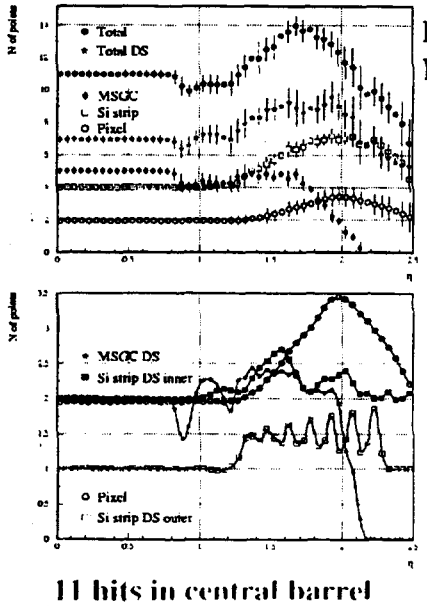
High Luminosity



13 hits in central barrel $|\eta| \leq 0.8$

8 Space points

Low Luminosity



11 hits in central barrel

6 Space points

Requirements

- Reconstruction of high P_t isolated tracks ($H \rightarrow ZZ^*$, W', Z', χ, °,$\chi^{\pm}$)
  - $\delta P_T/P_T \approx (15\ P_T \oplus 0.5)$ % for $|\eta| \leq 1.6$
  - $\delta\ P_T/P_T \approx (80\ P_T \oplus 0.5)$ % as $|\eta| \approx 2.5$

  } P_T in TeV range
- Muon momentum resolution
  - $\delta P_T/P_T \approx (4.5\ P_T \oplus 0.5)$ % for $|\eta| \leq 1.6$
- Hadron reconstruction (also important to establish isolation)
  - $\varepsilon \sim 95$ % for $P_T \geq 2$GeV
  - $\varepsilon \geq 85$ % for $1 < P_T < 2$GeV
- Impact parameter resolution (b /τ tagging $\Rightarrow$ Higgs, SUSY, $\not{CP}$)
  - δ d (r- ϕ)<25 μm over the full η range for P_T>10 GeV
  - δ d (z)<100 μm over most η
- Material
  - <53 % of $H \rightarrow \gamma\gamma$ with either γ converted in tracker

Pixel Requirements

- Provide two or more hits per track
  - ▶ Secondary vertices for b,c and τ tagging (Higgs, SUSY, B physics)
  - ▶ Reduce background of light quarks and gluons
- Help the pattern recognition at high luminosity
  - ▶ Confirm/reject track segments (≈25MB events with each beam crossing)
  - ▶ High precision extrapolation to vertex
  - ▶ Small occupancy in high multiplicity environment of heavy ions
- Performance
  - ▶ Sensors must operate up to $\phi = 6 \times 10^{14}$ hadrons/cm^2 at R=7 cm and provide sufficient charge
  - ▶ Readout analog block must operate with increasing $I_{leakage}$ and less Q. It must provide good S/N and time walk <25 ns
  - ▶ Readout architecture must minimize data loss of triggered bunch crossings

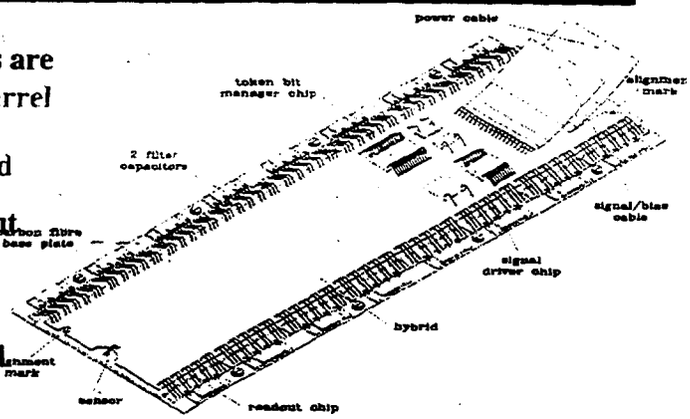
Modules

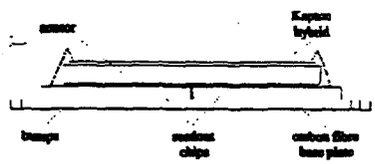
800 Modules in two configurations are the basic building blocks for the barrel

Sensors, 2× 8 readout chips, hybrid

carbon fiber plate glued to readout chip and attached to the cooling frame

Kapton cable supply clock, control signals, V_{bias} and send out hits





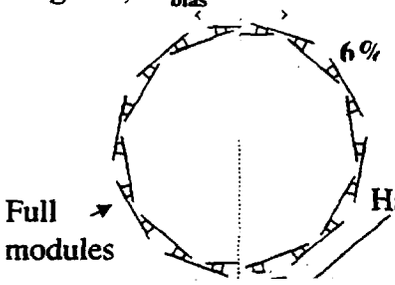
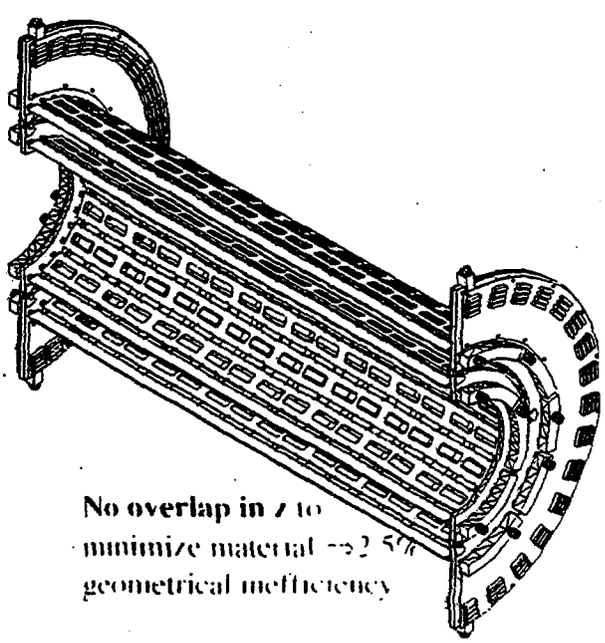


Plate 270 μm Chip 180 μm

Sensor 250 μm Hybrid 50 μ

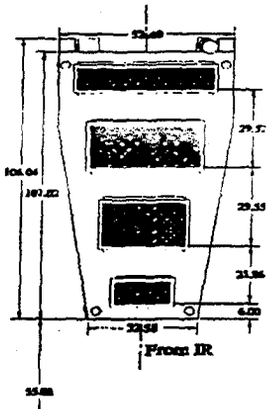
Barrel

- **Structural stiffness to provide stable pixel position O(10μm)**
- **Cooling must keep silicon T≤-10°C and remove 3kW**
- **Distortion due to ΔT must be <10 μm**
- **Material budget**
  - **Total Module 0.0101 X/X_0**
  - **Total cooling frame 0.0064 X/X_0**
  - **Total/layer 0.0165 X/X_0**
- **Must be built in two halves separated along a vertical line to accommodate pixel insertion scheme**



No overlap in z to minimize material ⇒2.5% geometrical inefficiency

End Disk Blades



5 different size of sensors with 2,5,6,8 and 10 chips

Segmentation in r allows to bias sensors receiving different doses separately

Overlap: 5% front back of blade, 4% adjacent blades 2% inefficiency due to imperfect overlap

96 Blades are the building blocks of Forward Pixel

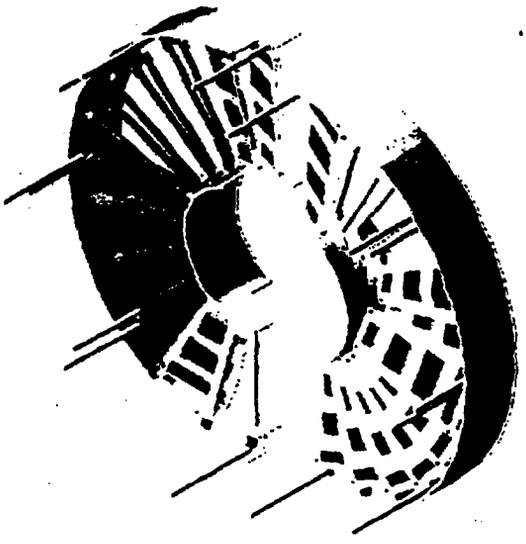
cooling tube: U shaped Al tube

A-frames high strength carbon fiber composite

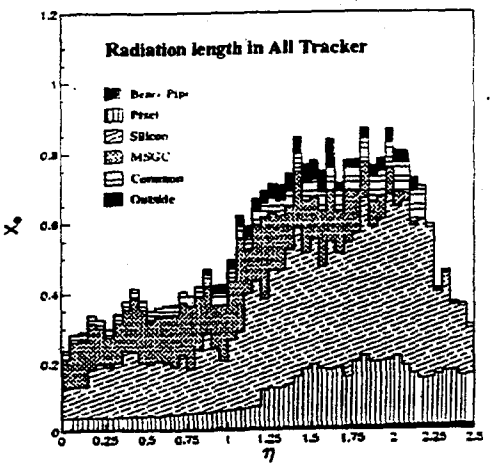
Tube and frames are gold plated and connected by dip brazing

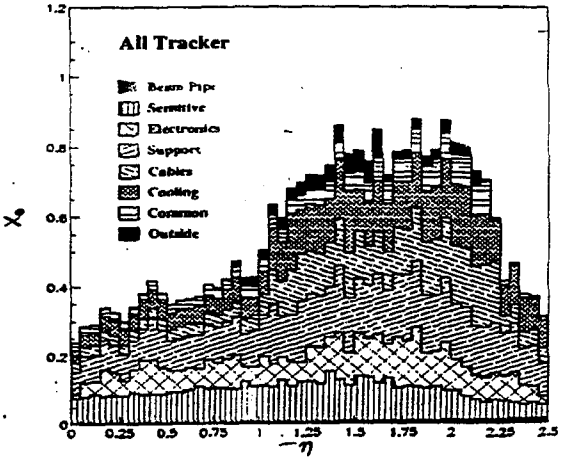
Turbine Geometry

- 12 Panel Support Structures are mounted between 2 half rings
- 20° rotation allows for charge sharing. Rotation is opposite for disks on different sides of IP
- Cooling supply and return lines are part of the space frame and service cylinder
- Material Budget
  - Panels 0.003 X/X_0
  - A frames 0.00316 X/X_0
  - Cooling pipes 0.00258 X/X_0
  - Total /wheel 0.023 X/X_0



Material





Constraints : Thermal screen between SST and MSGC.

Silicon tracker services require service to be axially at R=60 cm

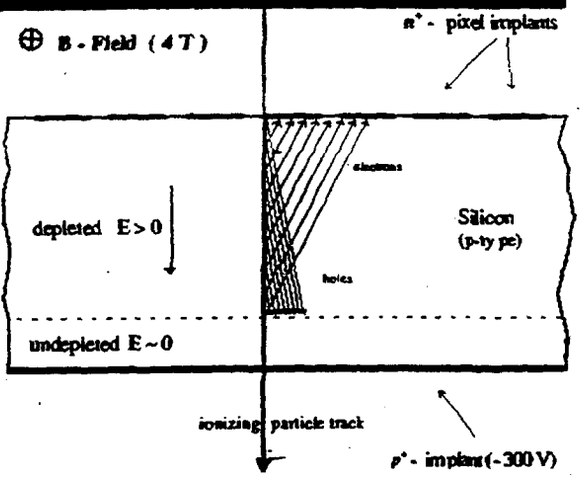
Installation of pixel sensor require services to be removed axially to the end flanges at R<20 cm

Cooling

- **Power consumption 60 μW/pixel⇒2.3 kW**
- **Total power 3kW**
- **Sensors must run at T=-10 °C**
- **Coolant should be**
  - **electrically isolating**
  - **inflammable**
  - **non-toxic**
- **HFE-7100 by 3M is a candidate but has radiation length=23cm**

Pixel size and shape

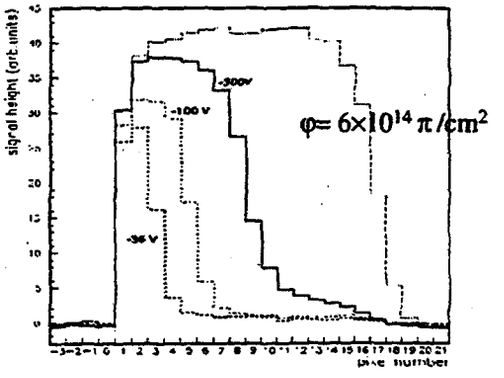
- Use n^+ on n-bulk silicon
  - ▶ Allows running with partially depleted sensors
  - ▶ large Lorentz angle in 4T field
- Impact parameter resolution depends on:
  - ▶ Hit resolution
  - ▶ Material budget
  - ▶ Distance from interaction region

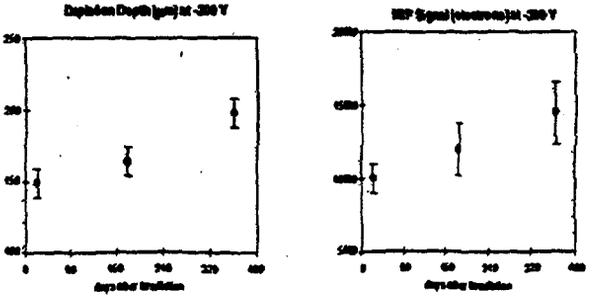


- Pixel size depends on: readout chip, dissipated power, cooling. Minimum pixel area needed to host chip is 0.015 $mm^2 \Rightarrow$ 120μm side $\Rightarrow$ 35 μm. Improve resolution by seeking charge sharing and analog readout $\Rightarrow$ side 150 μm to accommodate partial depletion .

Sensors R&D

- A 8 ×32 squared Pixel array (125 ~ μm side) was irradiated up to $\varphi = 3,6,9 \times 10^{14}$ π/cm^2 ($p(\pi)$=300 MeV/c) at T=3°C.
- Depletion depth measurement by the "grazing pions" method before and after irradiation.
- After irradiation sensors were kept at T=3°C. Annealing effects were observed after 6 and 12 months:
  - ▶ increase of the depletion depth
  - ▶ lower leakage current
- Expected signal 12000 e
  - ▶ Hit threshold 2000-3000 e
  - ▶ enc 400-600 e
  - ▶ $I_{leakage}$ =100 nA

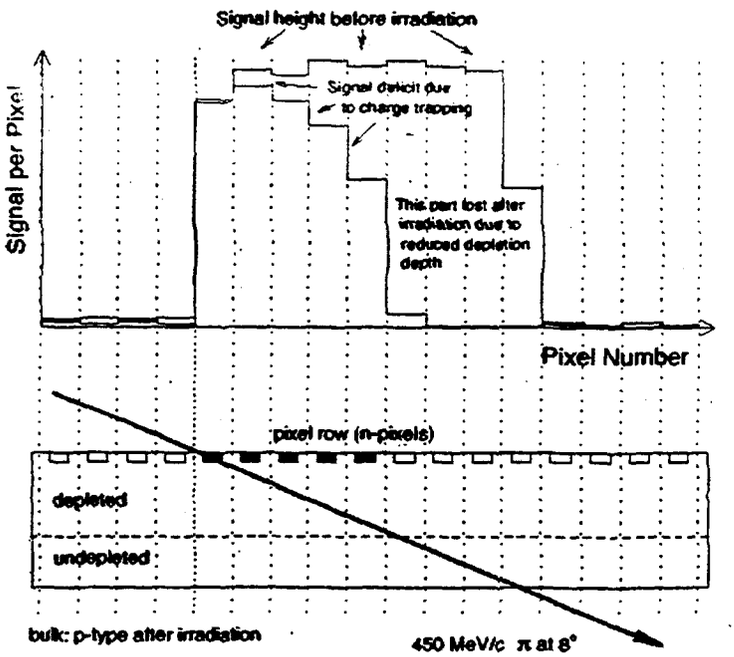




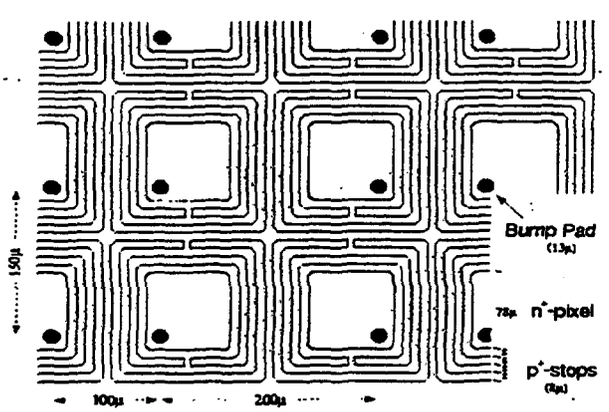
Grazing Method

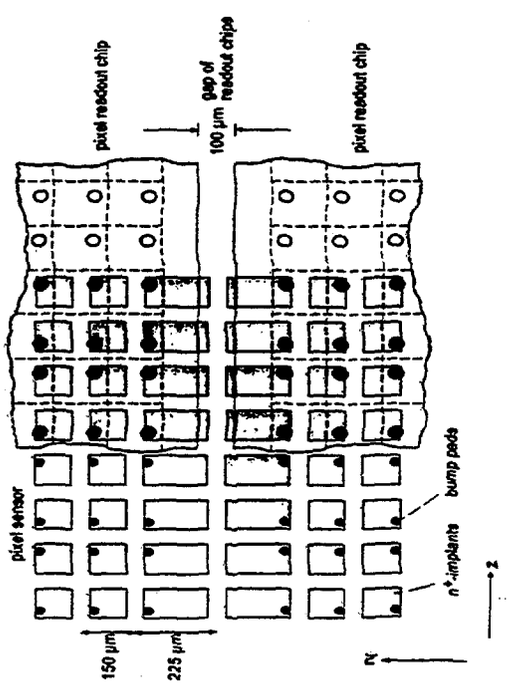
Signal from hit pixel measures the response at different depths

π graze pixel array at 8°



Sensors R&D





Pixels: 78 μm n-implants surrounded by two concentric p-stops rings with openings:

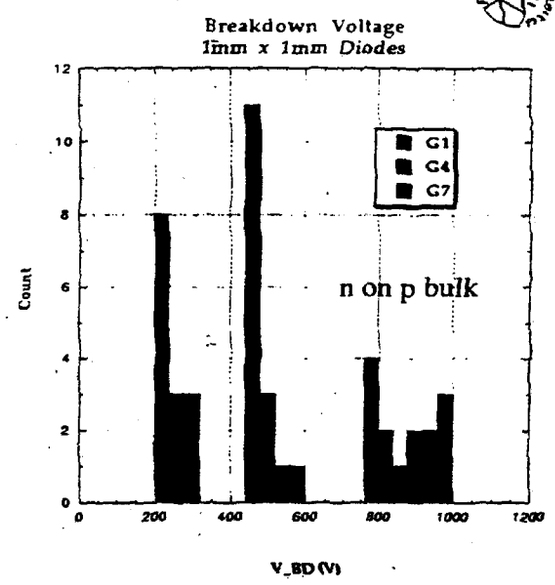
•high resistive path (O(100KΩ)) ⇒ Keep the n-implants biased if bump failed and allow $I_{leakage}$ testing before bump bonding.

•Reduce inter-pixel capacitance

Bump Pad =13 μm shifted by 25 μm to fit roc double column layout

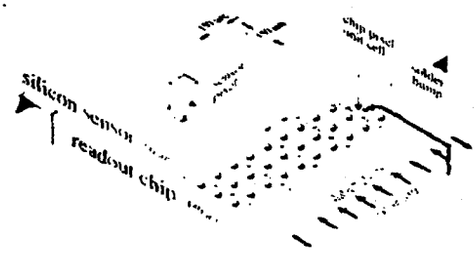
Sensors R&D

- Detectors must operate up to 300V. Breakdown voltage >500 V for $\varphi = 6\times10^{14}\,\pi/cm^2$
- Design with 7 guard rings have given good breakdown results.
- Avoid large ΔV between sensor and chip (15-20 μm gap)
- Comprehensive study of guard ring design is still going on

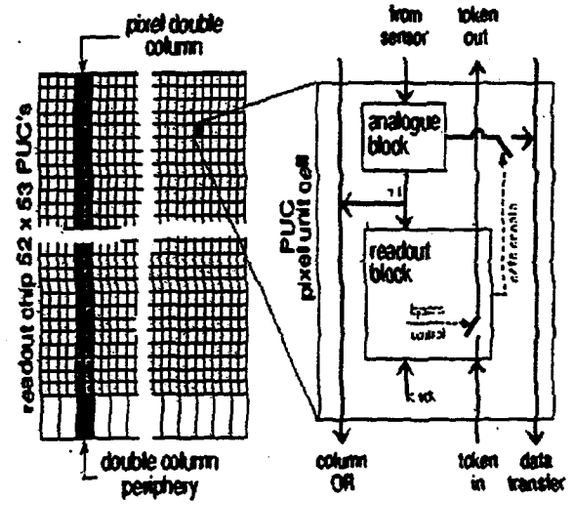


READOUT CHIP

Analog ROC



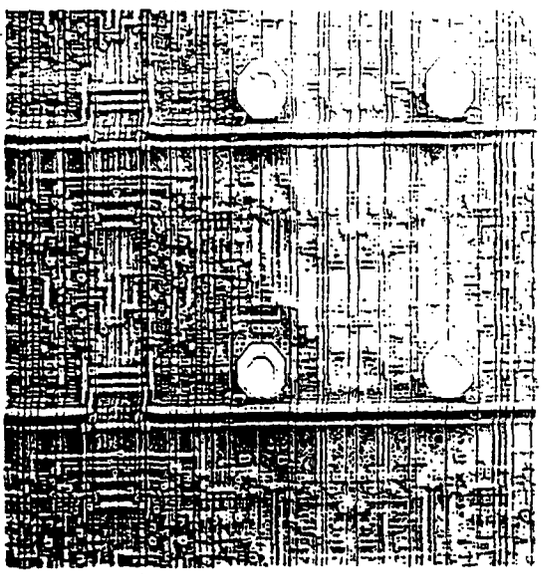
- Each pixel connected by a bump bond to Pixel Unit Cell (PUC)
- Double column architecture controlled by double column periphery
- Local bus lines connect all PUCC to column periphery (column Or)



- PUC analog block signal amplification
- PUC digital block transmit a pixel hit ASAP to column periphery

READOUT CHIP

- ROC and readout architecture design was guided by detailed *simulation of* sensors at the expected rates
- MC: PYTHIA top signal + 25MB. Low p_T tracks(>40 MeV/c) included. GEANT simulation included δ rays. ENC=300 e^- and 4 σ threshold.
- *Milestones:*
  - analog front end
  - choice of readout architecture
- Radiation hard prototype has been constructed and operated

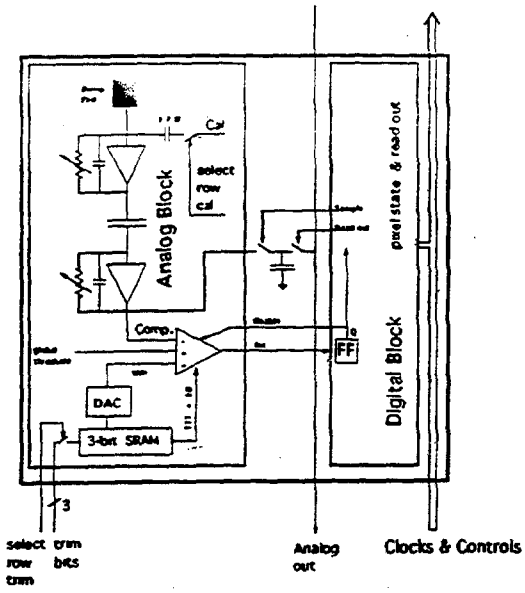


Pixel Unit Cell (PUC) Design considerations

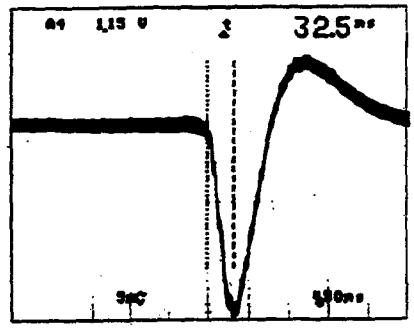
- Charge $Q_{initial}$=3fC down to 2.3 fC after 4 years at 7cm
- Increasing $I_{leakage}$ leads to:
  - additional noise $\propto$ to shaping time (average 50 e^- for 10 nA)
  - *sink leakage* current up to 100 nA because of large tails
- Low noise operation requires ENC < 500 e^-
  - minimize pixel capacitance (expect 80 fF for 150μm squared pixels)
  - minimize bump pad capacitance (15 fF)
- Rate of noise hits is function of threshold
  - Pixel to pixel variations require trim mechanism
- Minimize time walk for correct association of hit to bunch crossing
  - amplifier peaking time <25 ns (limit CMOS technology)
  - zero-level threshold
  - off line pulse height dependent time-walk correction
- Minimize crosstalk

Pixel Unit Cell (PUC)
Analog block

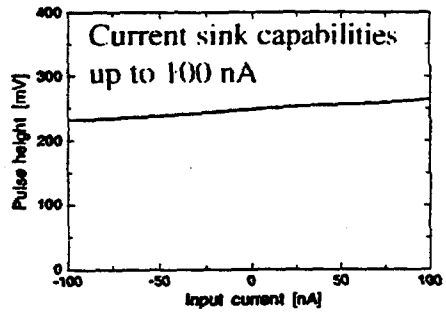
- Signal amplification: charge sensitive amplifier (feedback capacitor 30 fF) and capacitively coupled shaper⇒ gain=20-30 e/mV
- Hit detection: If signal > threshold PUC notifies periphery by column OR
- Global and trimmed threshold ⇒ Pixel masking and pulsing
- Temporary single hit storage

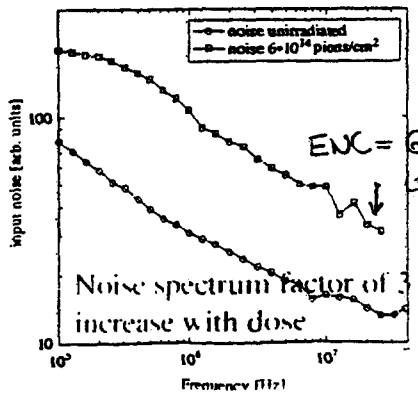


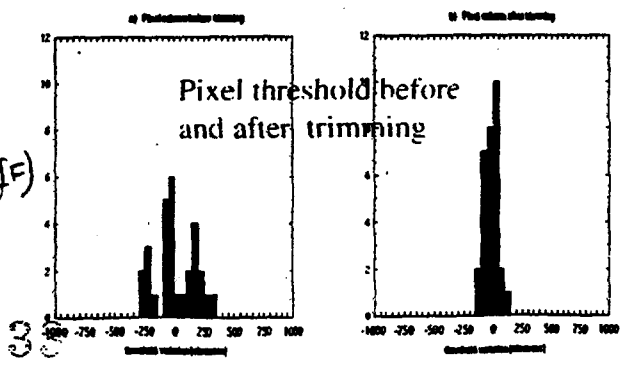
Pixel Unit Cell (PUC)
Prototype results



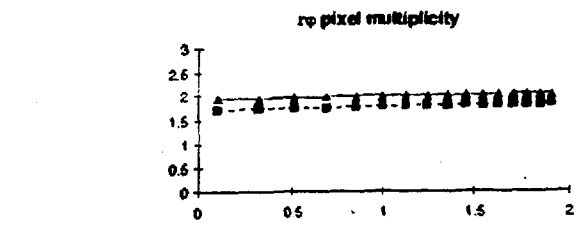
Signal pulse at the shaper output peak=32.5 ns with microprobe (100fF)

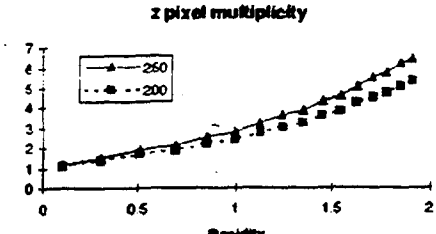


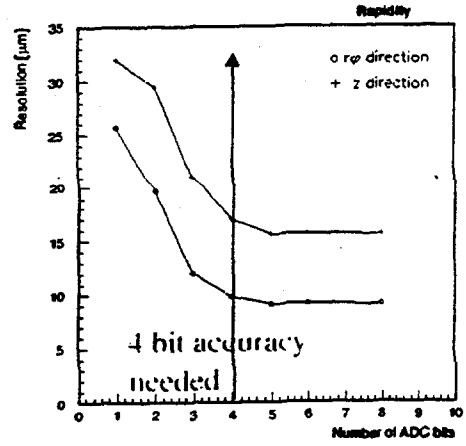


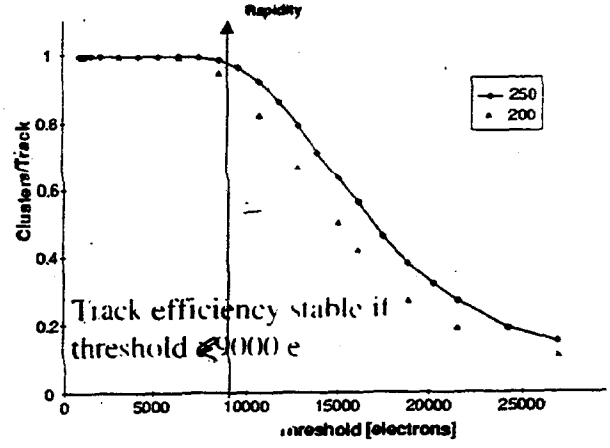


Pixel Unit Cell (PUC) Simulation results

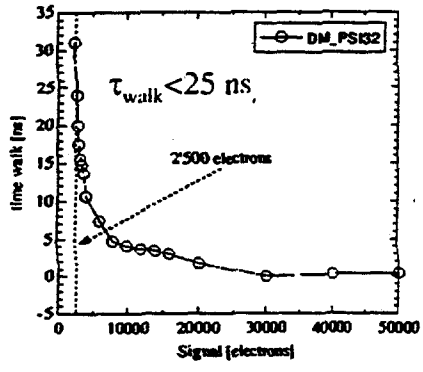


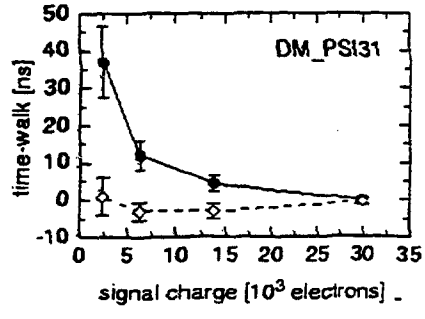




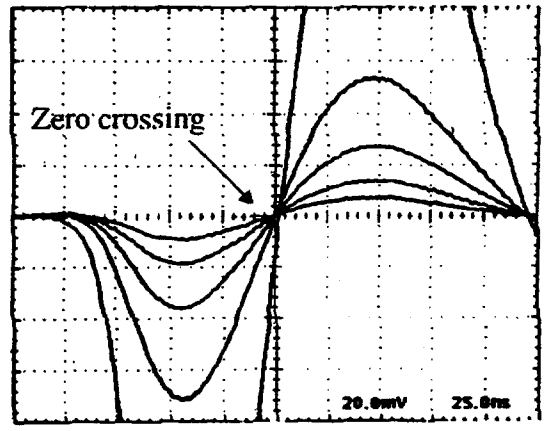


Pixel Unit Cell (PUC) Prototype results



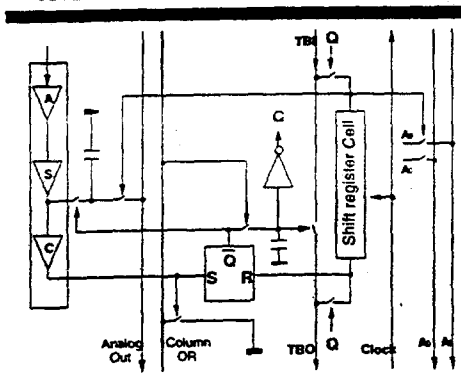


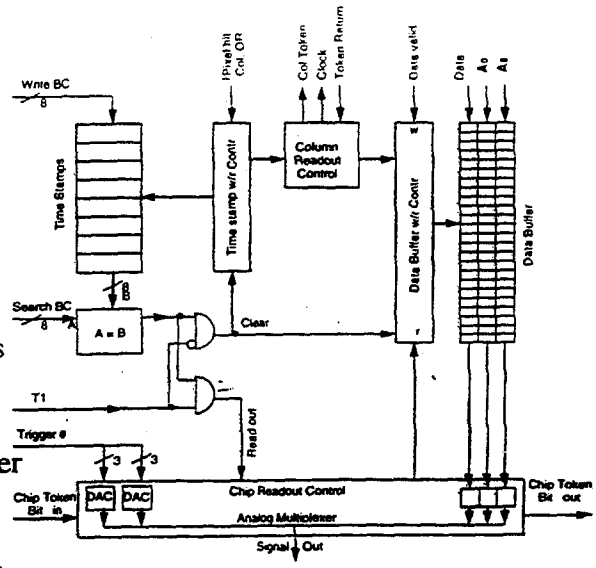
Amplifier pulses for different injected Q (1200-30000 e⁻) after irradiation with $10^{14}\pi/cm^2$



Implement pulse-height independent timing by using a second comparator

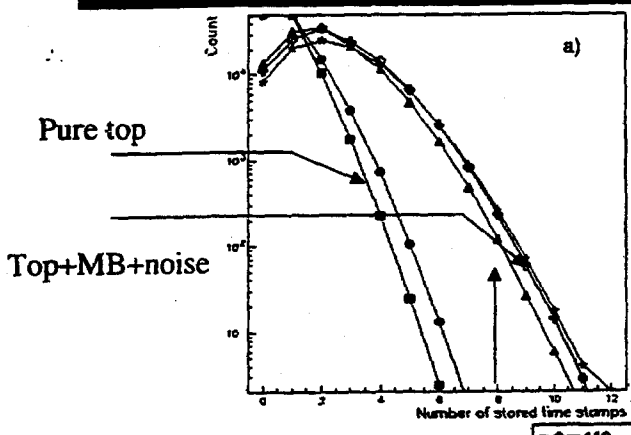
Column Drain Architecture

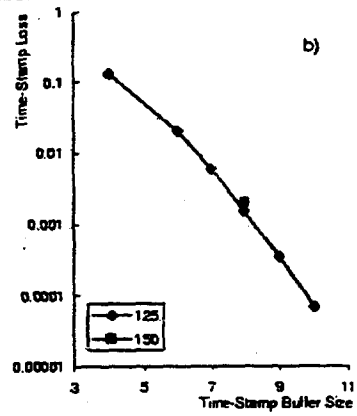


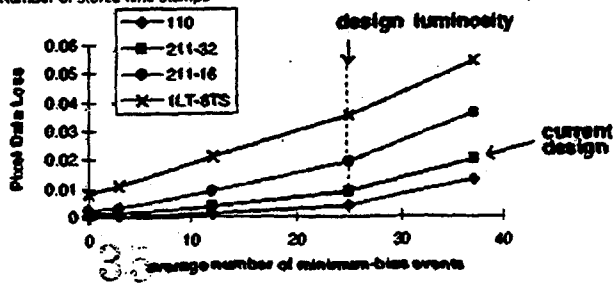


- The column periphery registers BC and sends token signal up and down the double column skipping empty pixels (at 1.6 GHz)
- In hit pixel the token signal initiate the transfer of pixel address and signal (Data Buffer) awaiting for L1T
- Time stamp, signal, addresses are transmitted from periphery to FED

Architecture Simulation



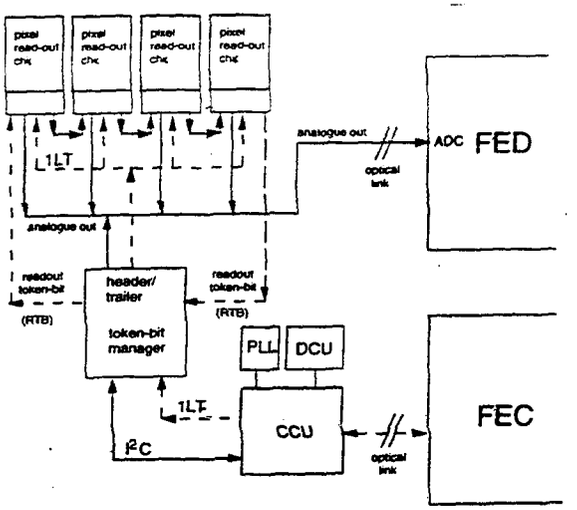




Architecture were pixel information stays on PUC until ITL is unacceptable

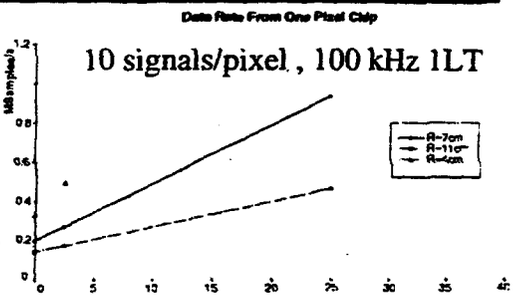
Data transmission

- Data accepted by 1LT is transmitted from column buffers to Front End Drivers located in the counting room.
- When and 1LT is present the Token bit manager chip (located on hybrid or portcard) puts a readout header signal on Analog-out bus and sends a readout token bit.
- RTB is passed through all the chips.



Data Rates

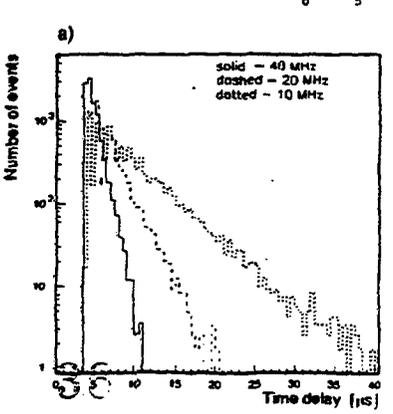
- High Luminosity a ROC will have one hit pixel/BC
- # of chips readout by a link must be chosen so that link does not saturate
- Assume analogue link will run ≥ 20 MHz

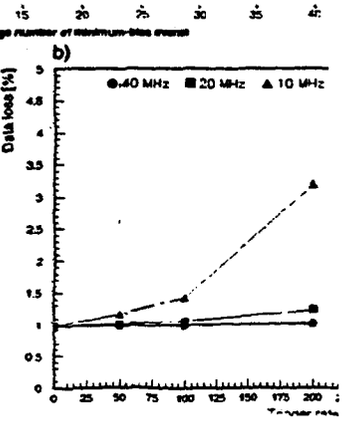


4 chip/link @7cm

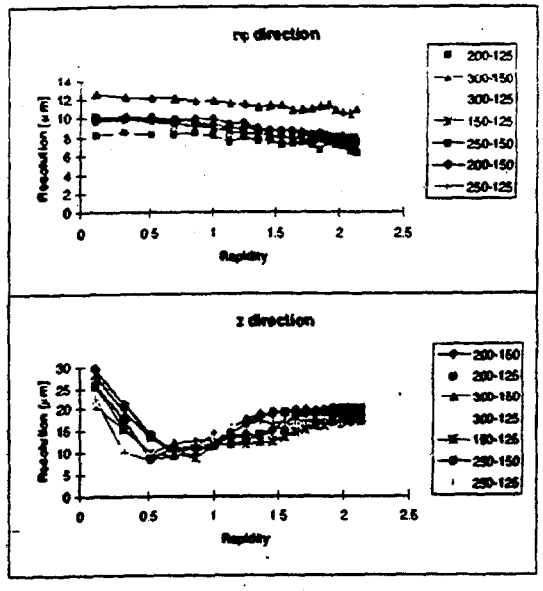
8 chip/link @11cm

<7chips>/link for endcaps

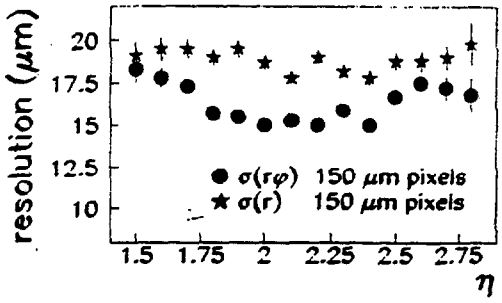




Hit Resolution



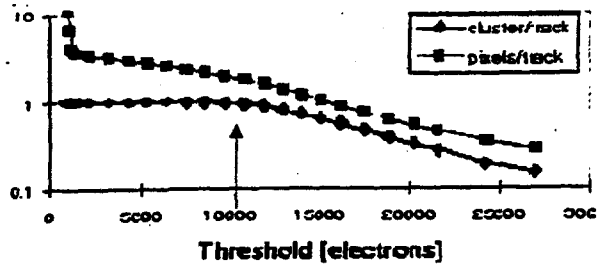
Hit Resolution for squared pixels as a function of the thickness and side length.



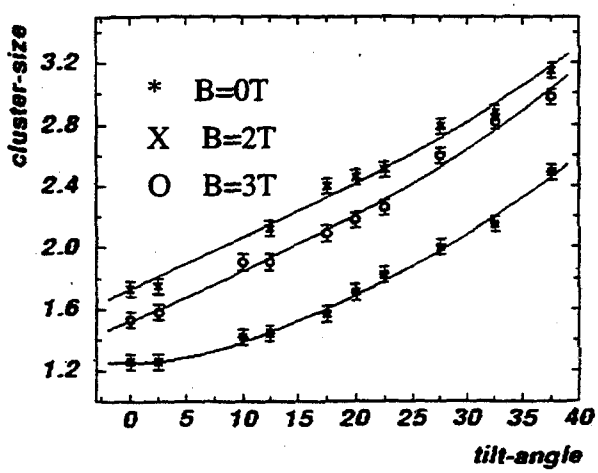
Endcap hit resolution

Hit Efficiency

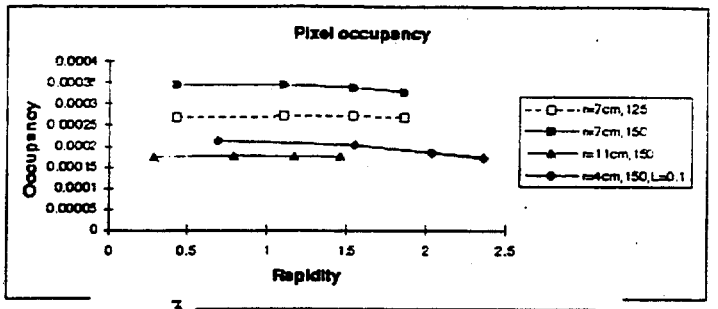
Cluster track efficiency ≈ 1 for threshold <10000e⁻

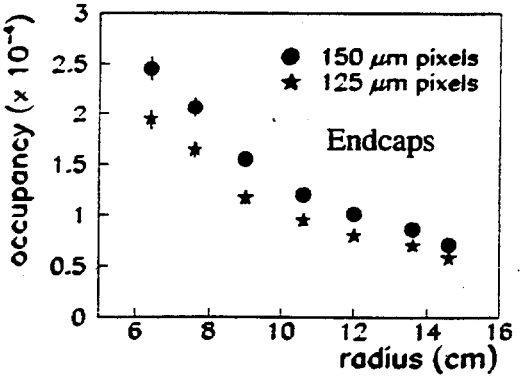


Measurements of 8×32 pixel array in B field (125 μm pixel side) agree with simulation



Occupancy





Barrel

Occupancy is defined as

$$n_{pixel} > 4\sigma/N_{total}$$

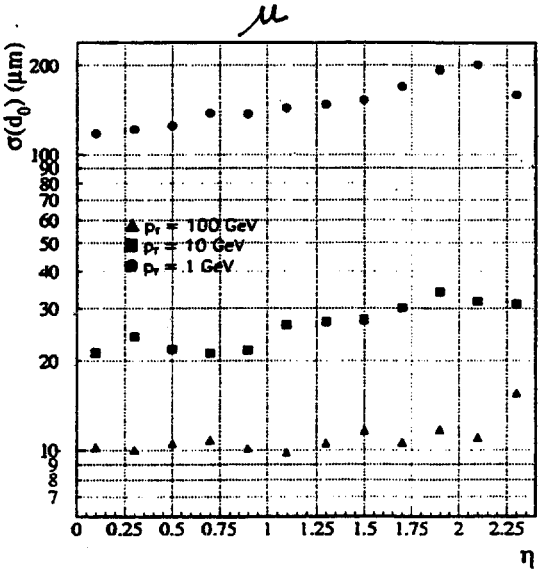
- **strong radial dependence influenced by B**
- **independent of η**

Performance

- **Impact Parameter resolution :**
  - **Dominated by the Pixel hit resolution and multiple scattering in the innermost pixel layer.**

    $\sigma(d0) \cong 9\ \mu m$ **for high** P_t
  - **In phase II the innermost layer is at 7 cm and**

    $\sigma(d0) \cong 12\ \mu m$ **for high** P_t



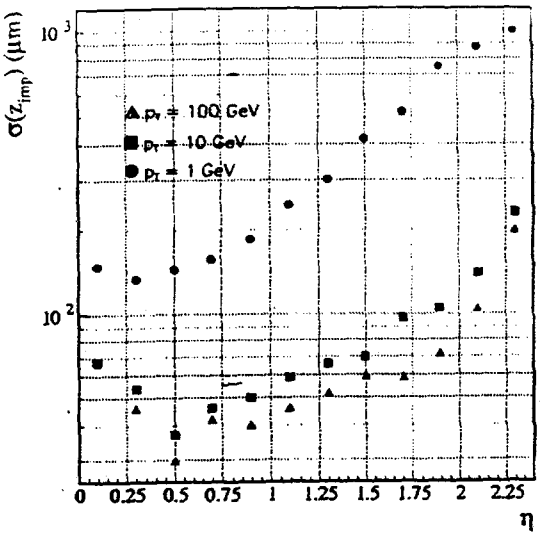
Performance

- Z_{imp} resolution:
  - At low P_T z_{imp} is degraded by multiple scattering and depends strongly on η

    $\sigma(z_{imp}) \approx 100\ \mu m$ central tracks

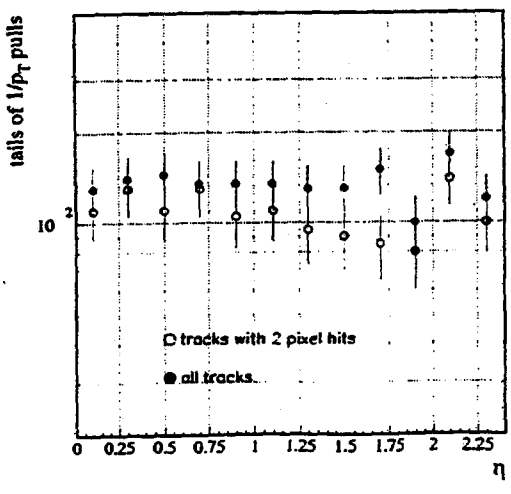
    $\sigma(z_{imp}) \approx 400\ \mu m$ at $\eta = 2$

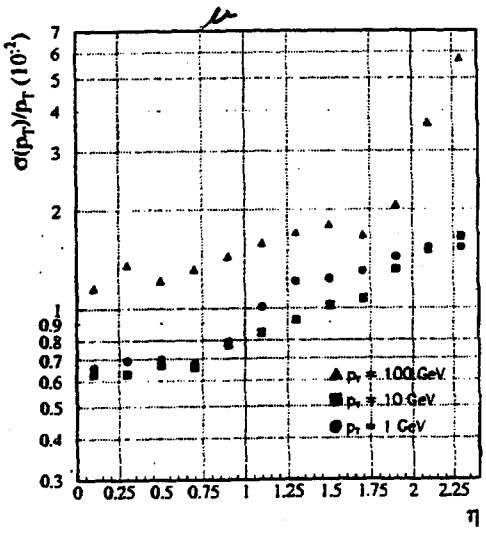
  - Further degradation in phase II since in Phase I barrel extend to $|\eta|=2.3$ while in phase II measurement is provided by endcap only



Performance

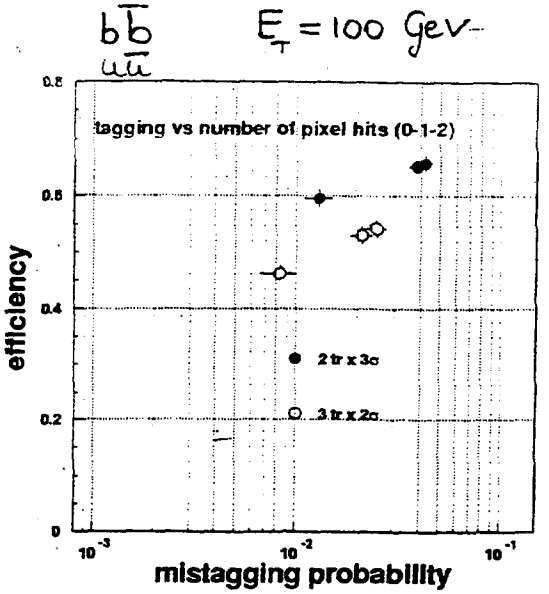
- P_T resolution:
  - 1-2 % for $|\eta| \leq 1.7$
  - Degradation at higher $|\eta|$ because of smaller tracker lever arm





B-tagging

- Impact parameter Tagging Efficiency as a function of mis-tagging rate for 100 GeV jets:
  - Phase I has a higher b-jet efficiency since the pixel layer is closer to beam pipe
  - At least 2 measurements in the pixel detector are necessary to achieve high quality



Summary

- Pattern recognition and track reconstruction quality are achieved at high Luminosity
- Sensors R&D shows that operation at high voltage is feasible
- Novel p-stop design should minimize capacitance and allow to keep pixels at V if bump bond fails
- Radiation-hard Prototype chip achieves performance within the LHC requirements

  Pixel threshold of 2500 e^- is above cross talk level

  A 5σ cut requires noise level of 500 e

- Prototypes power dissipation is within the analog power budget of 40 μW/pixel

Federico Antinori (INFN-Padova)
for the Alice Collaboration

Silicon Pixels in Alice

Alice Pixels Institutes:
Bari, Catania, CERN, Padova, Roma, Salerno

Contents:

- Introduction:
  Alice, why Si pixels, requirements
- Bird's eye view of basic concepts and status of R&D for:
  - Ladder assembly
  - Front-end chip
  - System r/o and control
  - Bussing
  - Mechanics & Cooling

→ see also related talks:

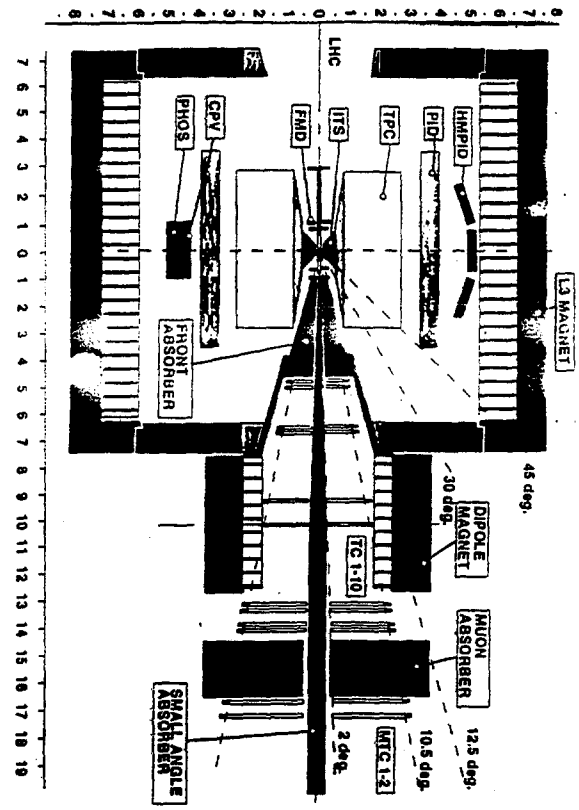
- E. Cantatore on RD19/WA97/NA57
- W. Snoeys on front-end chip
- W. Klempt on Alice Inner Tracking System mechanics

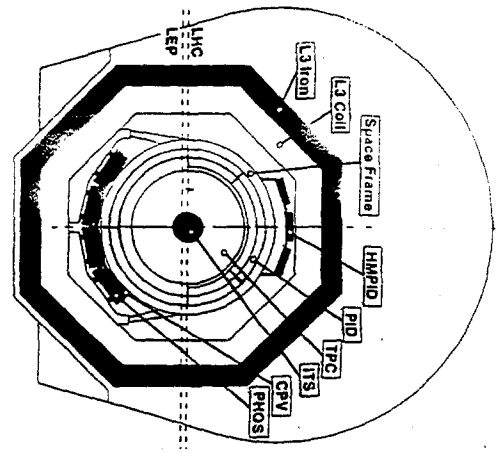
Alice environment

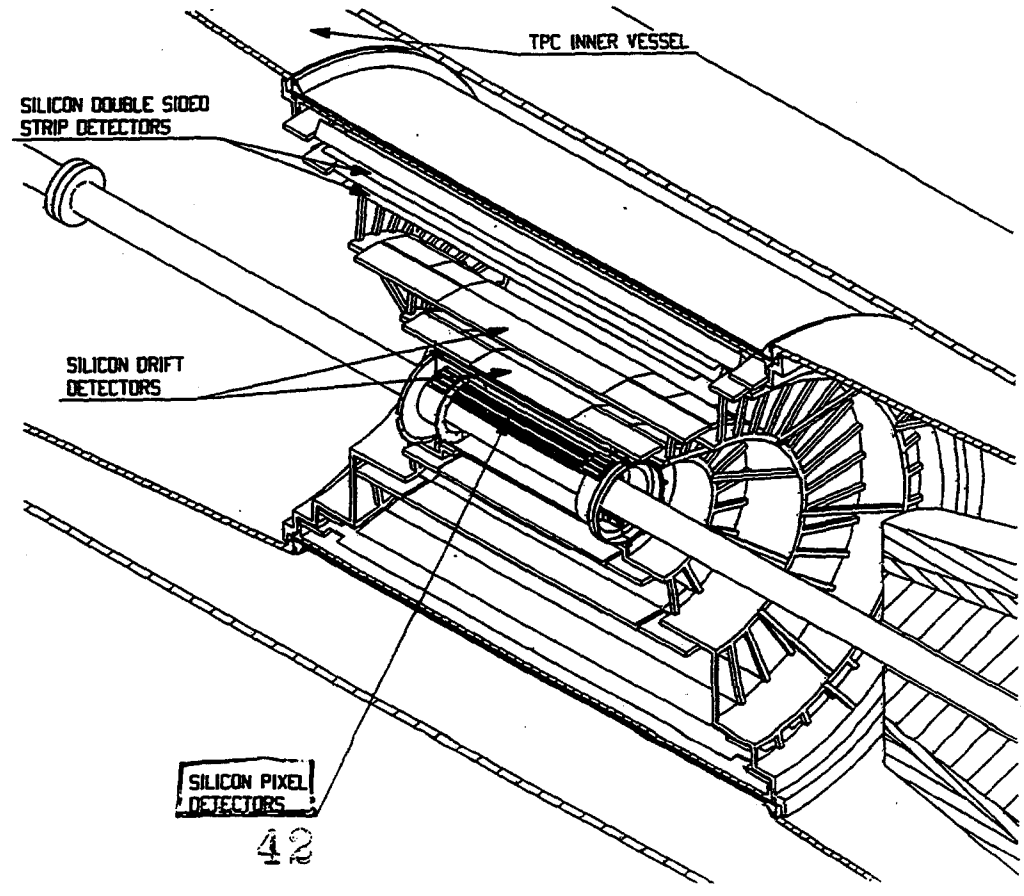
Nucleus-Nucleus collisions at $\sqrt{s}$ = 5.5 TeV/nucleon
☞ search for deconfinement phase transition
hadronic matter → Quark-Gluon Plasma (QGP)

	Pb+Pb	p+p	Ca+Ca (low)	Ca+Ca (high)
L ($cm^{-2}s^{-1}$)	10^{27}	10^{30}	$2.7\ 10^{27}$	10^{29}
Rate (kHz)	8	100	8	300

Radiation:
at ~ 4 cm from beam in 10y standard running scenario:
200 krad, 10^{12} n/cm^2


LHC
PHOS
CPV
FMD
ITS
TPC
PID
HMPID
L3 MAGNET
FRONT ABSORBER
45 deg.
30 deg.
DIPOLE MAGNET
TC 1-10
MUON ABSORBER
12.5 deg.
10.5 deg.
2 deg.
MTC 1-2
SMALL ANGLE ABSORBER


LHC
LEP
L3 Iron
L3 Coil
Space Frame
HMPID
PID
TPC
ITS
CPV
PHOS


TPC INNER VESSEL
SILICON DOUBLE SIDED STRIP DETECTORS
SILICON DRIFT DETECTORS
SILICON PIXEL DETECTORS

Si Pixels in Alice

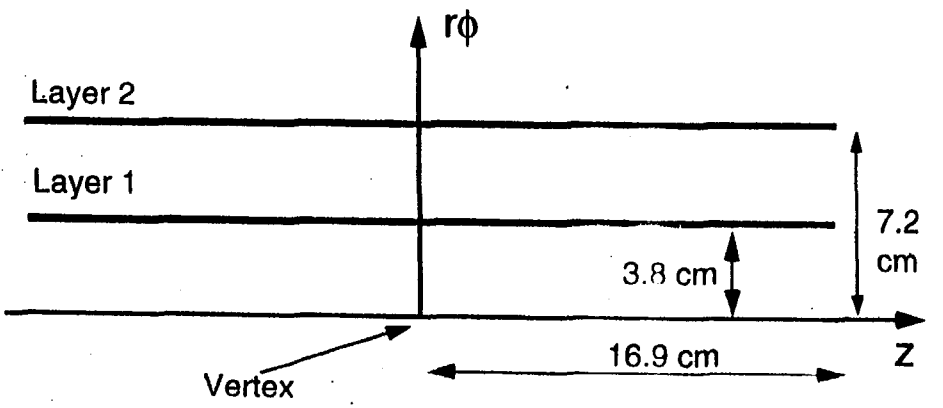
→ Two innermost layers:

- Mainly for secondary vertex detection (strangeness, charm)
- Less than 10 cm from the vertex
- Track density > 50/cm^2

☞ Need high precision, high double track resolution → Si pixels!

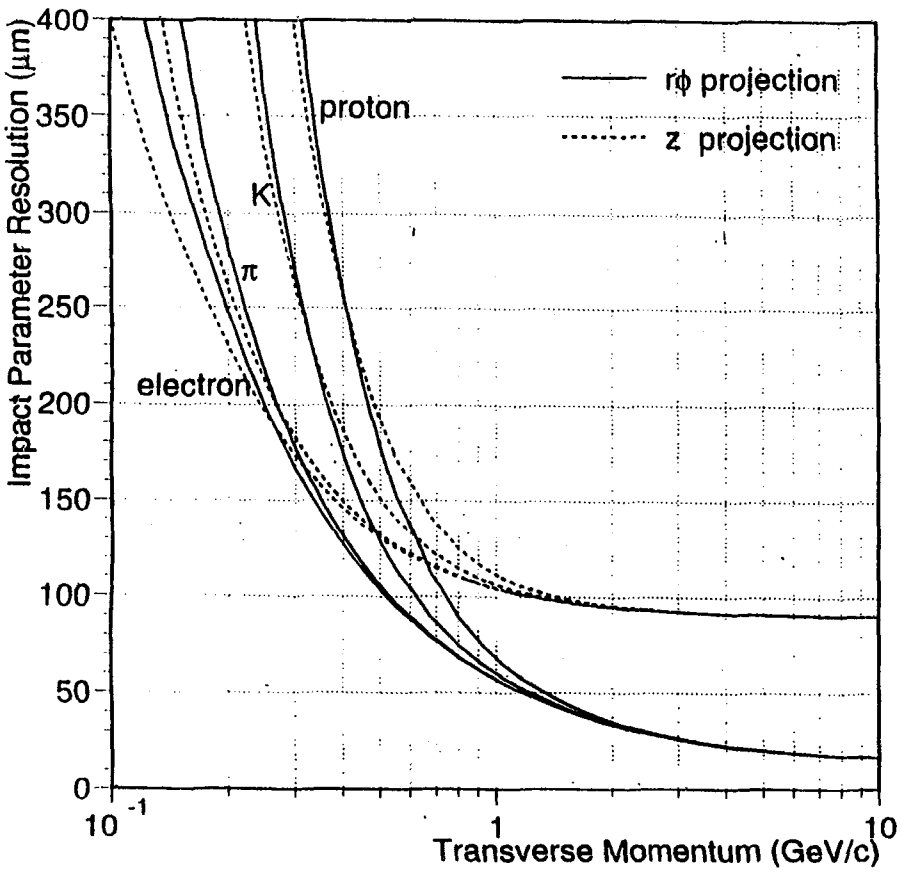
→ High rate capability can be exploited in high luminosity running modes, e.g. standalone determination of primary vertex position for Debye screening runs (~ 500 kHz in Ca+Ca collisions at L=10^{29} cm^{-2} s^{-1})

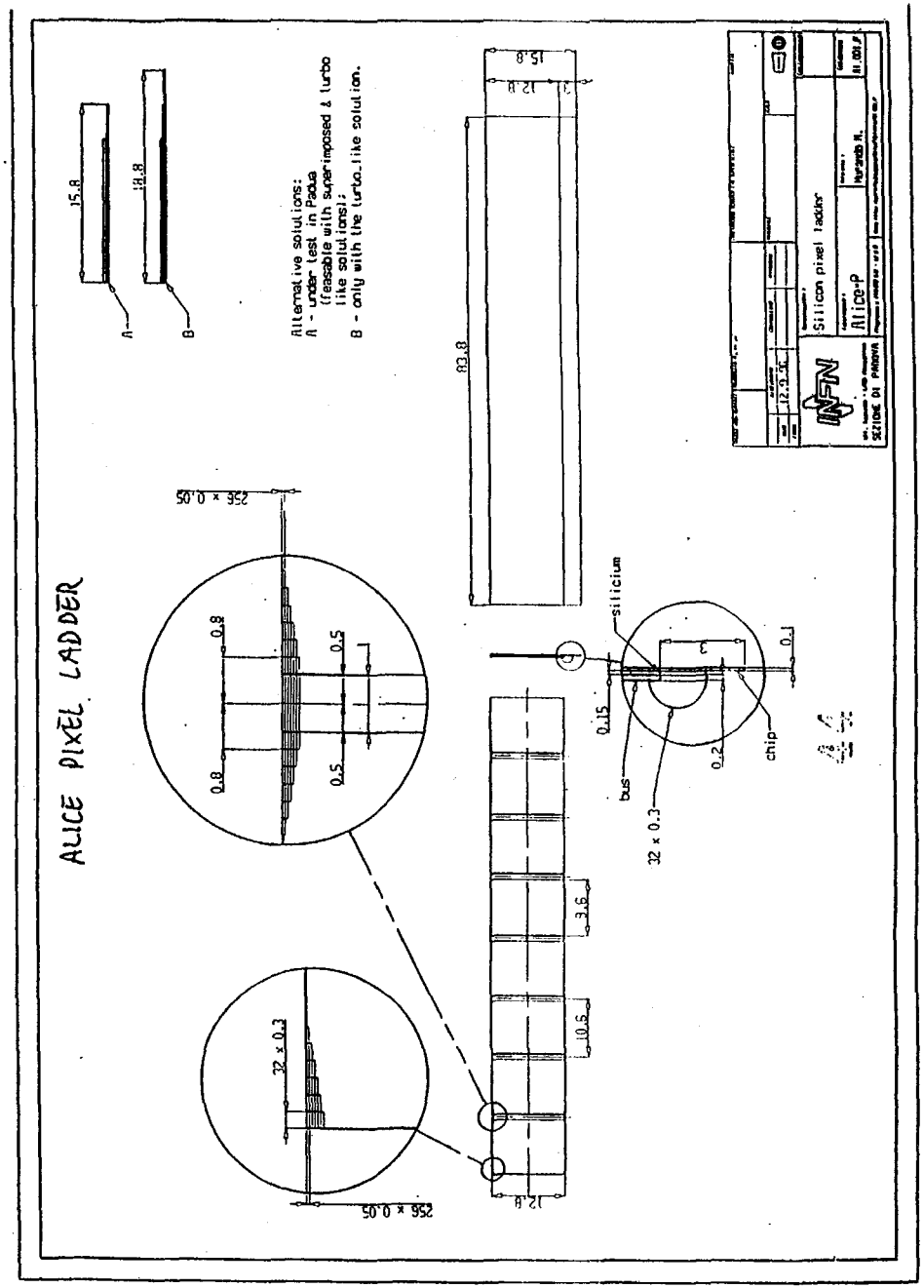
Requirements



- cell size: 50 μm (rϕ) x 300 μm (z)
- strobe latency: up to 2.5 μs
- strobe duration: 200 ns
- r/o speed: < 200 μs / event
- material thickness: ~ 0.6 % X_0 / layer
- radiation tolerance: 200 krad, 10^{12} n/cm^2

Impact Parameter Resolution





Bump-bonding

- Production of Omega3 assemblies for NA57 experiment ongoing with GEC-Marconi
- 1.2 M pixels installed in the NA57 telescope
- In the present production we have reached a ladder yield of ~ 70%

Thin assembly

- Thinned-down chip (100 µm) and thin detector (150 µm) Omega3 wafers at GEC-Marconi, ready for bump-bonding

Front-end chip specs

- Cell size: 50 µm (critical) x 300 µm (non critical)
- Binary read-out
- Strobe latency: 2.5 µs
- Strobe duration: 200 ns
- R/O time (system): 200 µs
- Rad tolerance: > 200 krad
- Threshold: 2000 e with 200 e spread (thin detector)
- Individual chip bias adjustments with on-chip DACs
- JTAG controls
- Individual cell mask at digital level + column mask
- 32 x 256 cells per chip

LHC2 Test / Alice1Test chip (CERN-MIC group)

2 x 65 cells in MIETEC 0.5 µm:

- Gate-all-around design for rad tolerance
- individual cell leakage current compensation

☞ rad tolerance at least several 100 krad
→ OK for Alice

but:

- density still insufficient for full Alice cell implementation in 50 µm x 300 µm
- relatively large threshold variation

→ see presentation by Walter Snoeys

Alice2Test chip (CERN-MIC group)

2 x 65 cells in IBM 0.25 µm, ready for submission

improvements w.r.t. Alice1Test:

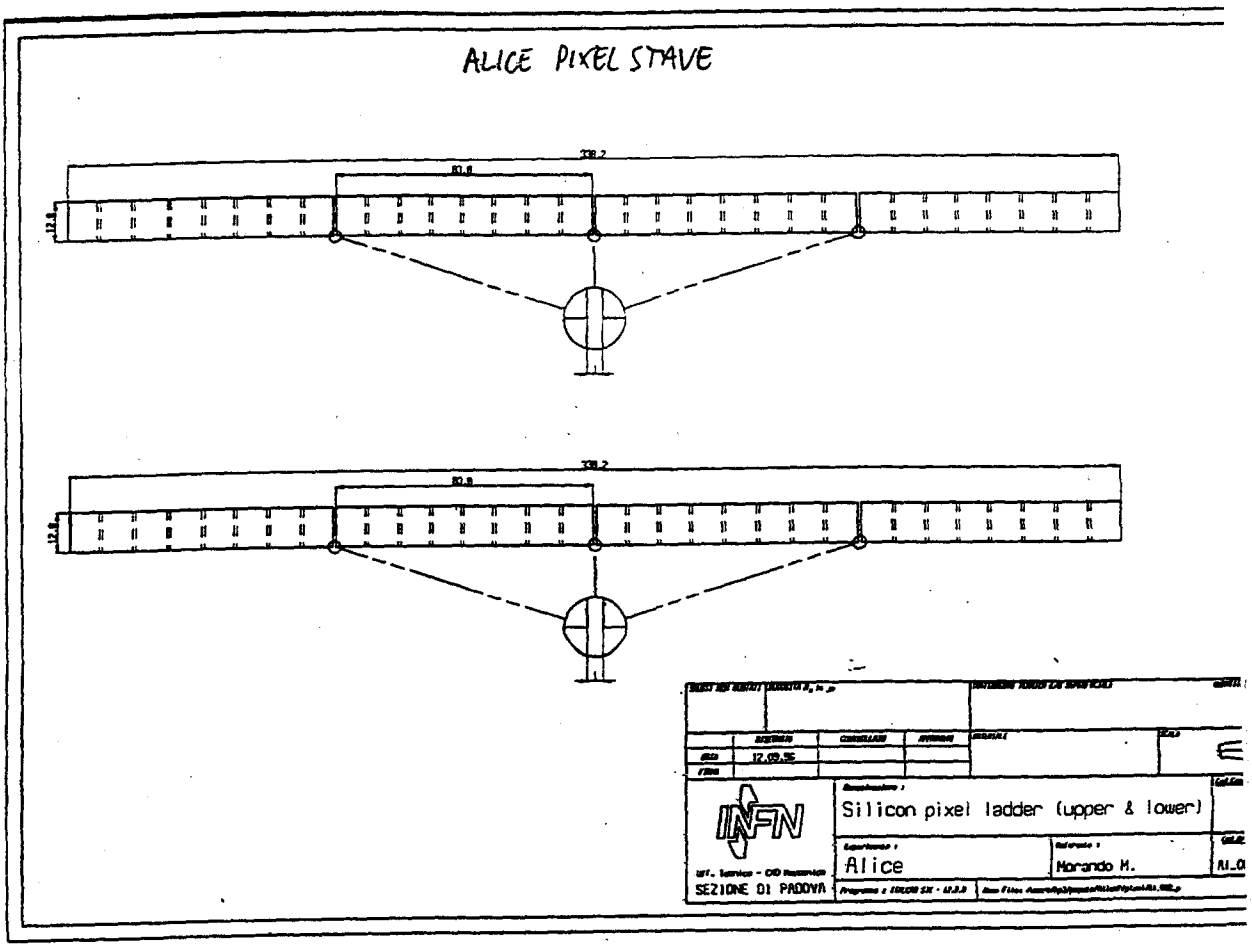
- higher density (→ still higher radiation tolerance?)
- no nMOS current mirrors (better use of real estate)
- counter replaces delay line

→ density sufficient for full Alice cell implementation in 50µm x

- individual cell 3-bit threshold adjust

→ see presentation by Walter Snoeys

☞ full-size Alice chip being designed, submission at end of 199



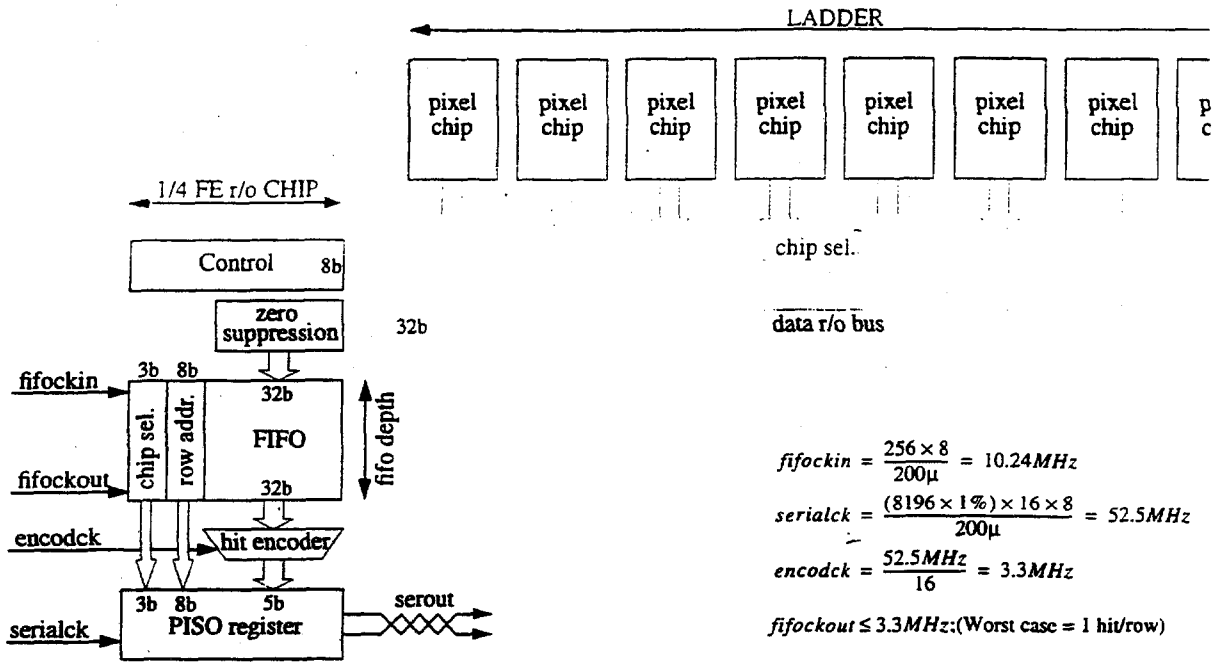
System r/o and control: (CERN - ED group)

Basic principles:

- Readout in 200 μs → 10 MHz clock row shift
- Minimize cabling → serial link (+ buffering)
- Minimize data on link → zero suppression, address encoding
- Simple control + testability (boundary scan) → JTag - IEEE 114
- High integration → custom control chip at end of the stave (rad. tolerant like front-end chip)

Readout block diagram.

- *The basic modularity for the Readout is the Ladder.*



$$fifockin = \frac{256 \times 8}{200\mu} = 10.24MHz$$

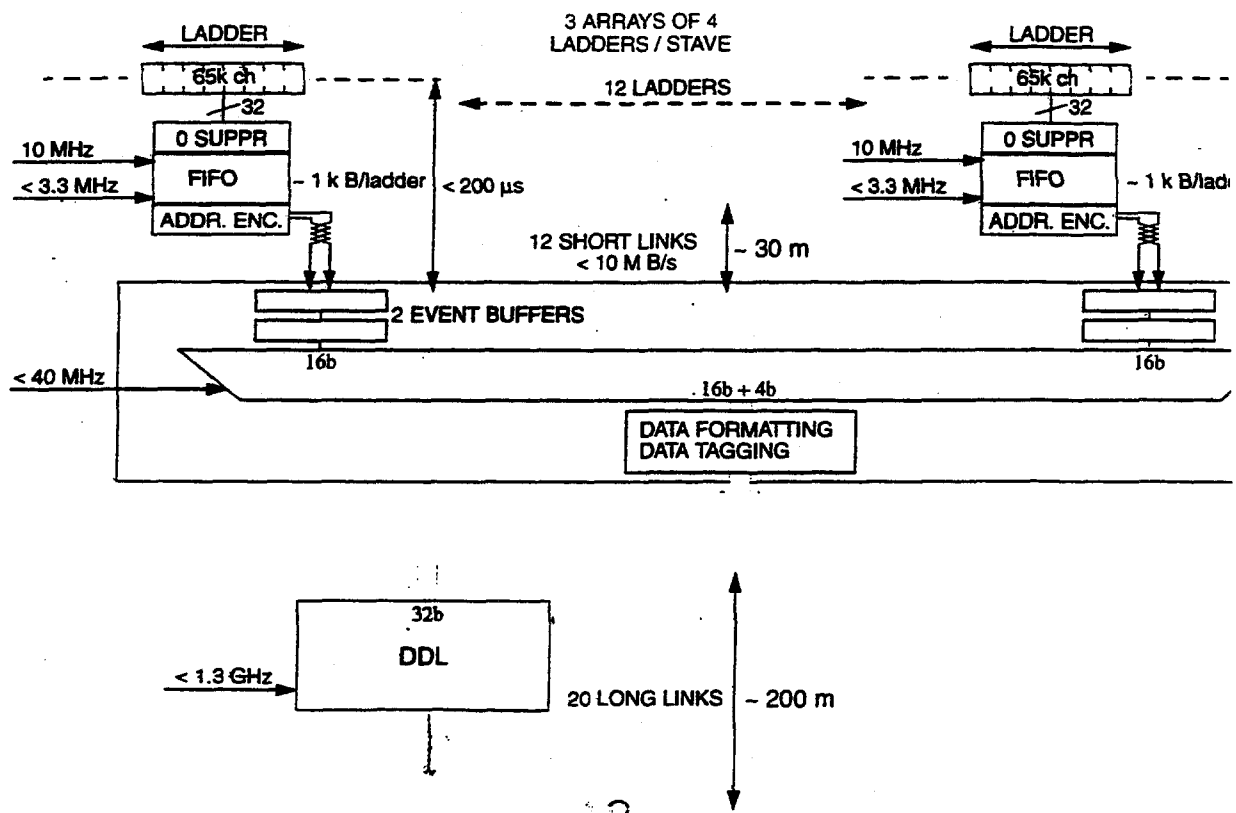
$$serialck = \frac{(8196 \times 1\%) \times 16 \times 8}{200\mu} = 52.5MHz$$

$$encodck = \frac{52.5MHz}{16} = 3.3MHz$$

$$fifockout \leq 3.3MHz\text{:(Worst case = 1 hit/row)}$$

$$fifodepth = R(n \geq 1) \times 8 = 70 \times 8 = 560w$$

Readout by DDL.



Bussing

Read-out and control bus:

- Multi-layer (~5)

- thin (~10 μm Al, ~ 20 m polyimide per layer)

- 100 to 150 μm line pitch.

- CERN workshop → down to ~ (<) 200 μm line pitch → OK for Omega3 ladders

We are:

- producing an Omega3 version to learn how to handle these circuits on the present ladders

- contacting vendors, preparing a market survey
  → from informal contacts:
  150 μm pitch feasible now,
  100 μm pitch in 1-2 years

Mechanics, cooling
(INFN - Padova)

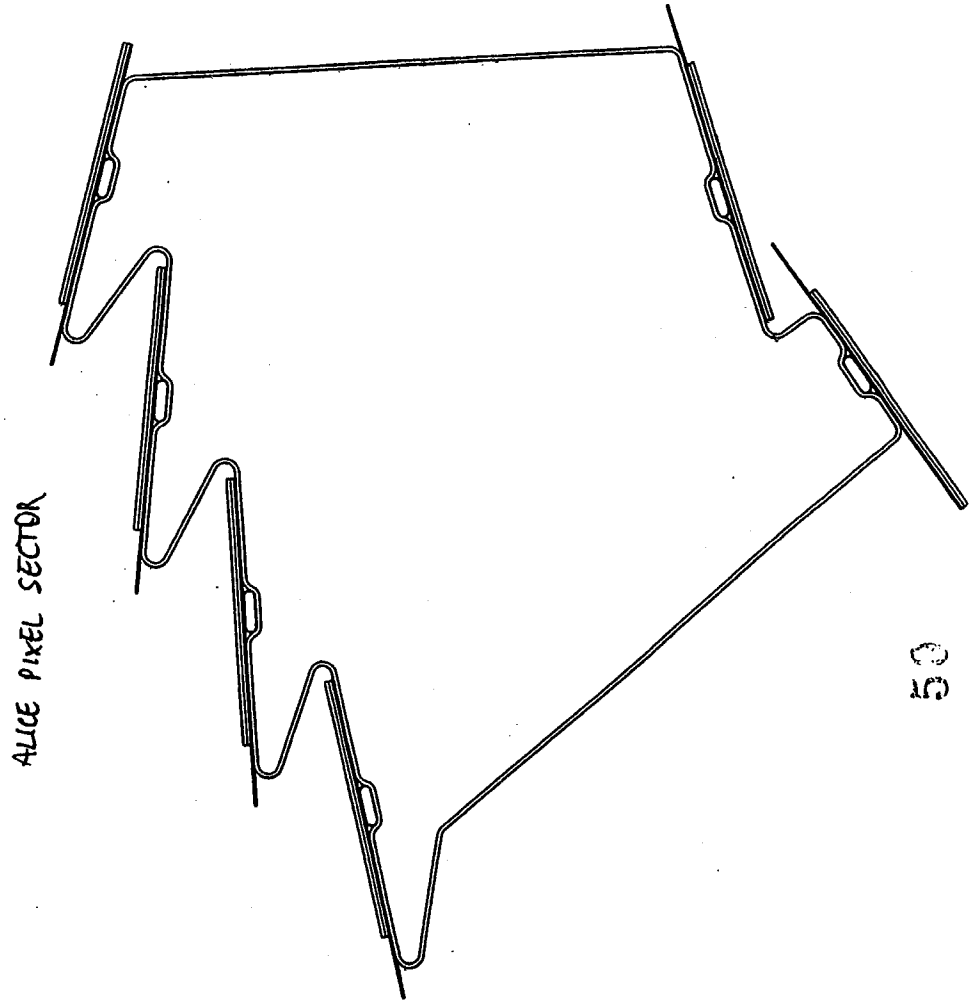
Basic choices:

- Material:
  - minimize radiation length
  - high modulus
    → unidirectional carbon fibre
  - optimize thermal and mech. properties
    → cyanate resin
  - maximise fibre/resin ratio
  - adapt material to geometry

- Geometry:
  - minimize material for required stiffness
  - reasonable modularity for maintenance
    → 10 independent support sectors
  - maximise ladder support surface
    → turbo solution

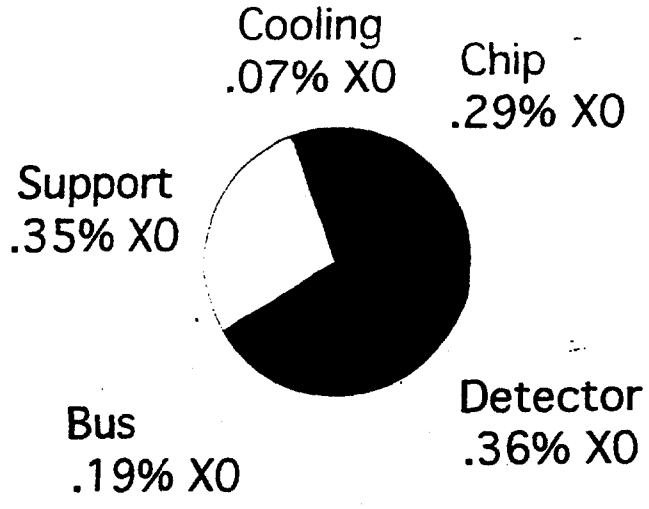
Basic choices, contd:

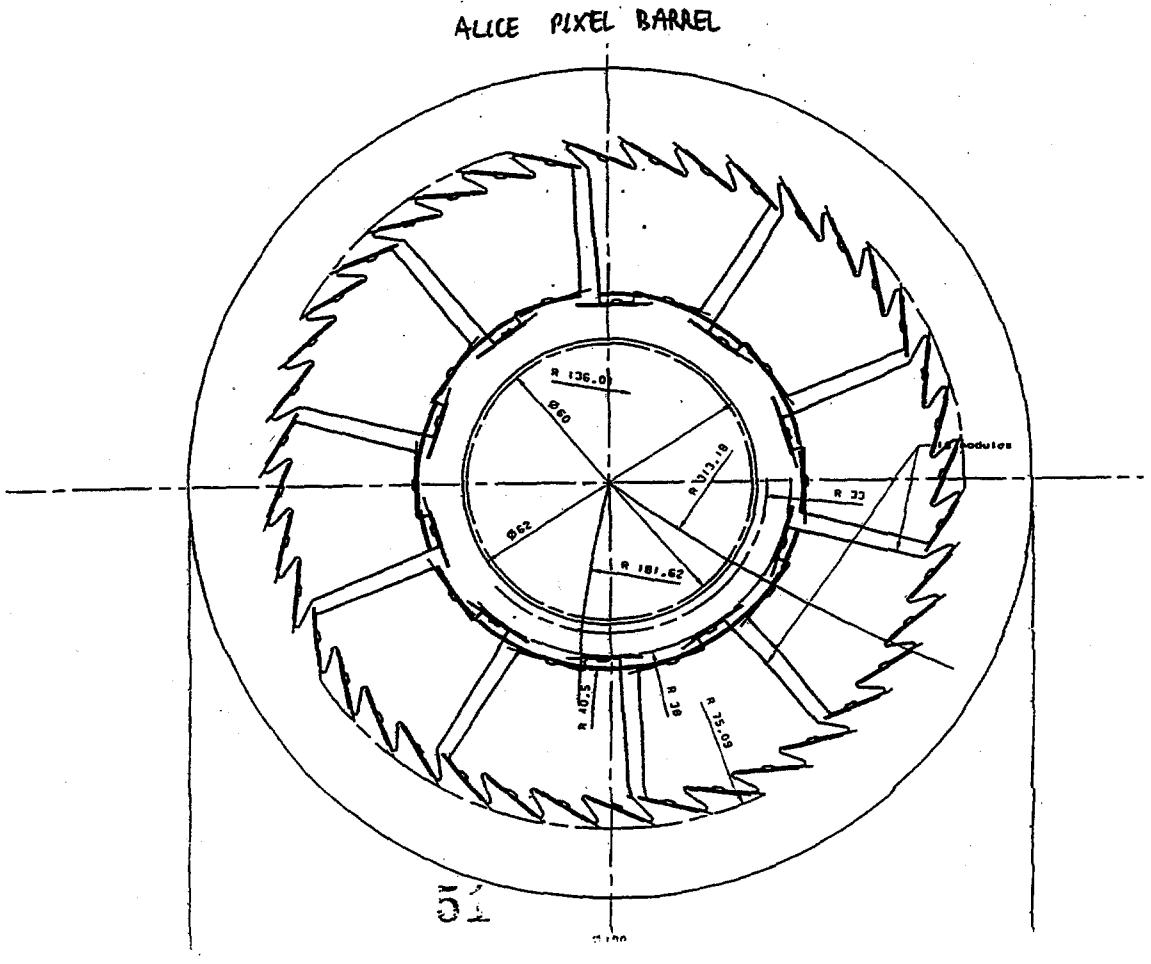
- Cooling:
  - No need to go below room temperature
  - W_{TOT} ~ 500 W
    → air cooling is out
  - Minimise fluid density
    → water cooling
  - Robustness w.r.t. plumbing faults
    → "leakless" (below 1 Atm)
  - Maximise exchange surface
    → squeezed cooling vessel
  - Integrate cooling vessel in carbon fibre structure



Material Distribution

Average material seen by a particle traversing both layers = 1.26% X0





Mechanics, cooling R&D
(INFN Padova)

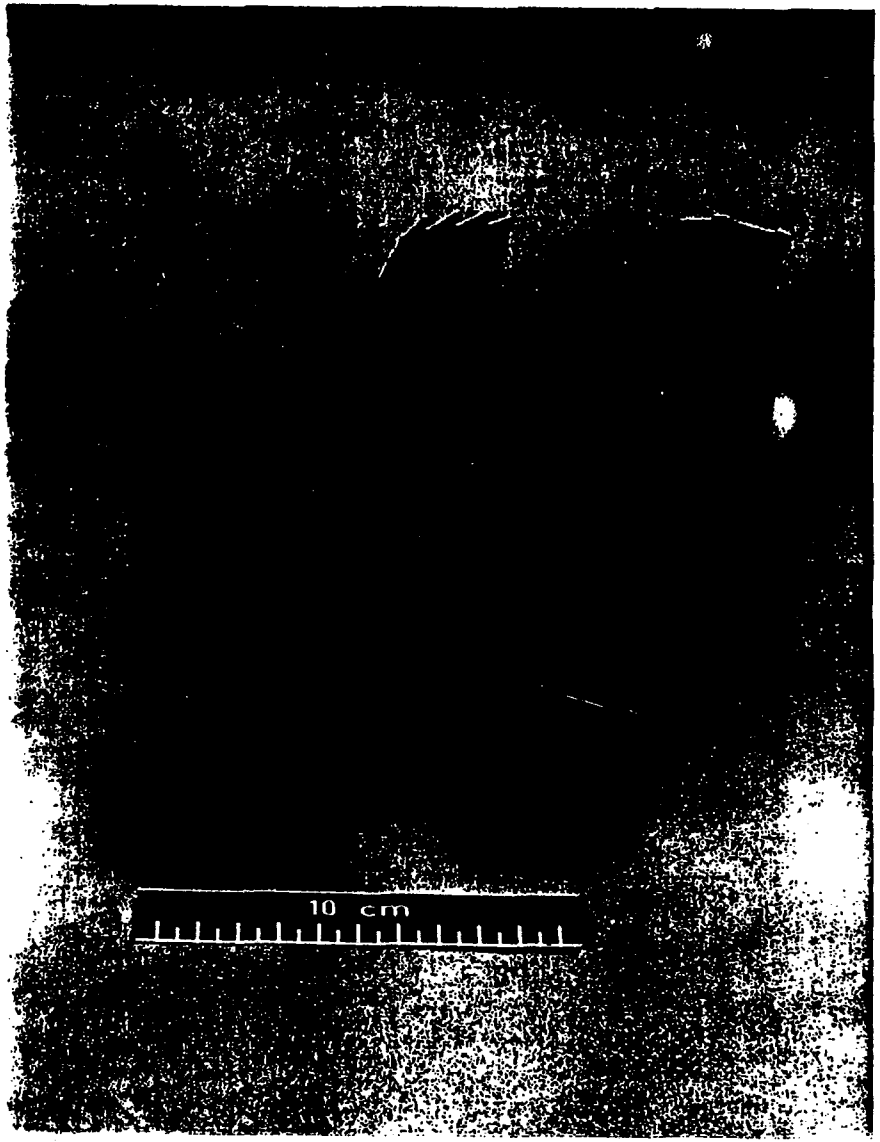
- Full-size prototypes of carbon-fibre support sectors produced in industry

→ <u>feasibility demonstrated</u>

- Composite material lab at LNL (Legnaro) now operational → next phase in-house

- Setting up "leakless" cooling system in LNL

- To do:
  - study/control stability of production tolerances
  - control local buckling
  - verify cooling simulations



Main Design Parameters

		Layer 1	Layer 2
r		3.8 cm	7.2 cm
Δz		33.8 cm	33.8 cm
cell size	50 μm x 300 μm		
# cells	15.7 M	5.2 M	10.5 M
occupancy		1 %	0.3 %
# ladders	240	80	160
surface	0.26 m^2	0.09 m^2	0.17 m^2
strobe latency	2.5 μs		
strobe duration	200 ns		
min. threshold	2000 e		
threshold rms	200 e		
r/o time	200 μs		
power	~ 500 W	~ 150 W	~ 350 W
total thickness	1.2%X_0	.6% X_0	.6%X_0
det. thickness	150 μm		
chip thickness	100 μm		
rad. tolerance	200 krad, 10^{12} n/cm^2		

International Pixel Detector Workshop
PIXEL98
May 7-9, 1998
Fermilab, Batavia, Illinois

Developments of Pixel Hybrid Photon Detectors for the RICH counters of LHCb

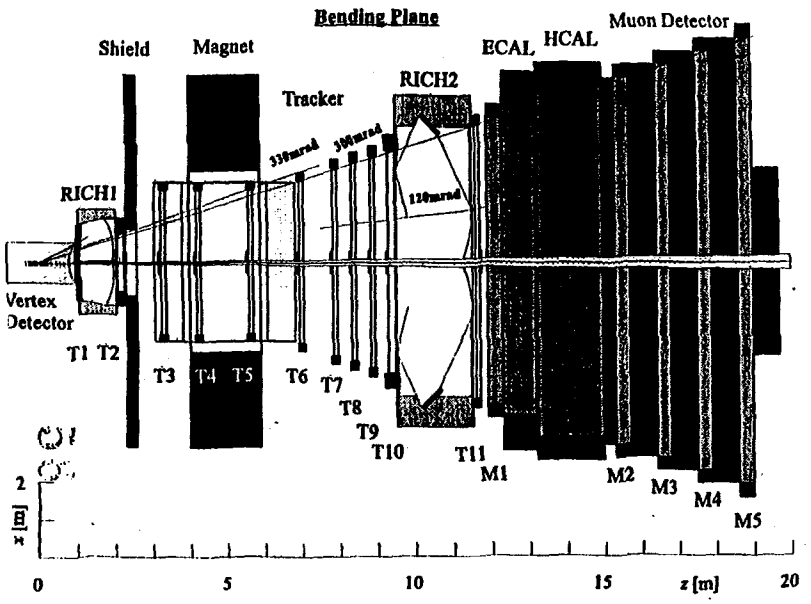
M. Alemi[1,2], M. Campbell[1] (speaker),
F. Formenti[1], T. Gys[1],
D. Piedigrossi[1], D. Puertolas[3],
E. Rosso[1], W. Snoeys[1], K. Wyllie[1]

1 CERN, Geneva, Switzerland
2 University of Milano, Italy
3 INFN Section of Rome, Italy

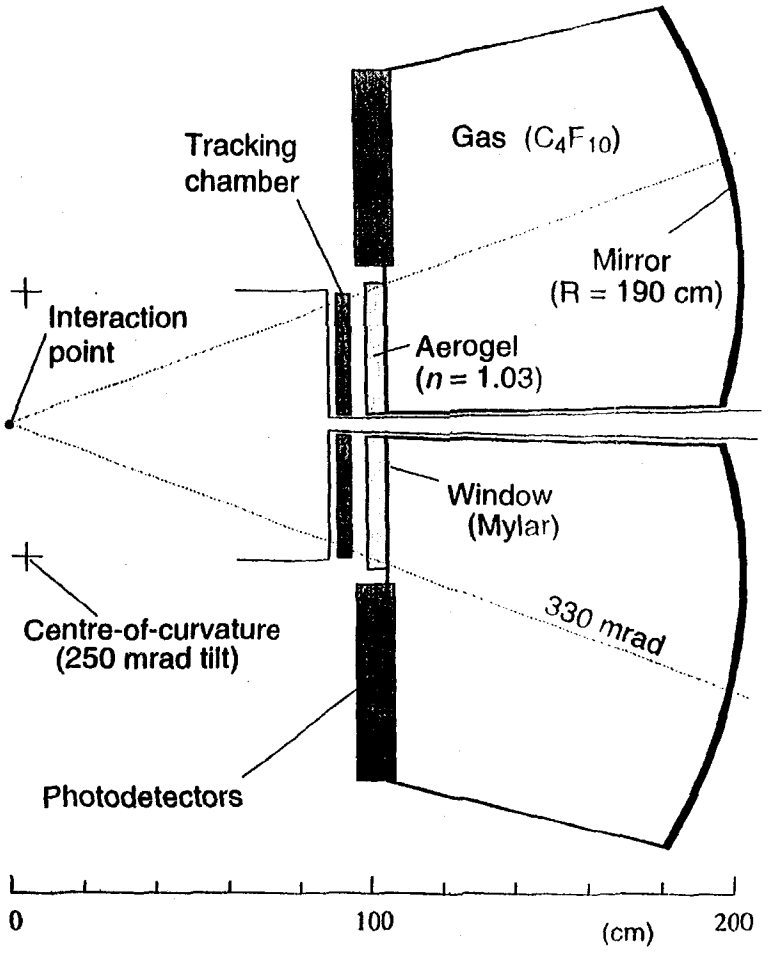
Outline of the talk

- **Introduction**
  - The LHCb RICH counters
  - Overall system requirements
  - Photo-detector requirements
- **Half-scale prototype tube**
  - Schematic design
  - Single-photoelectron efficiency
- **Large tube developments**
  - Schematic design
- **Front-end and read-out electronics**
  - Architecture
  - Implementation
- **Conclusions**

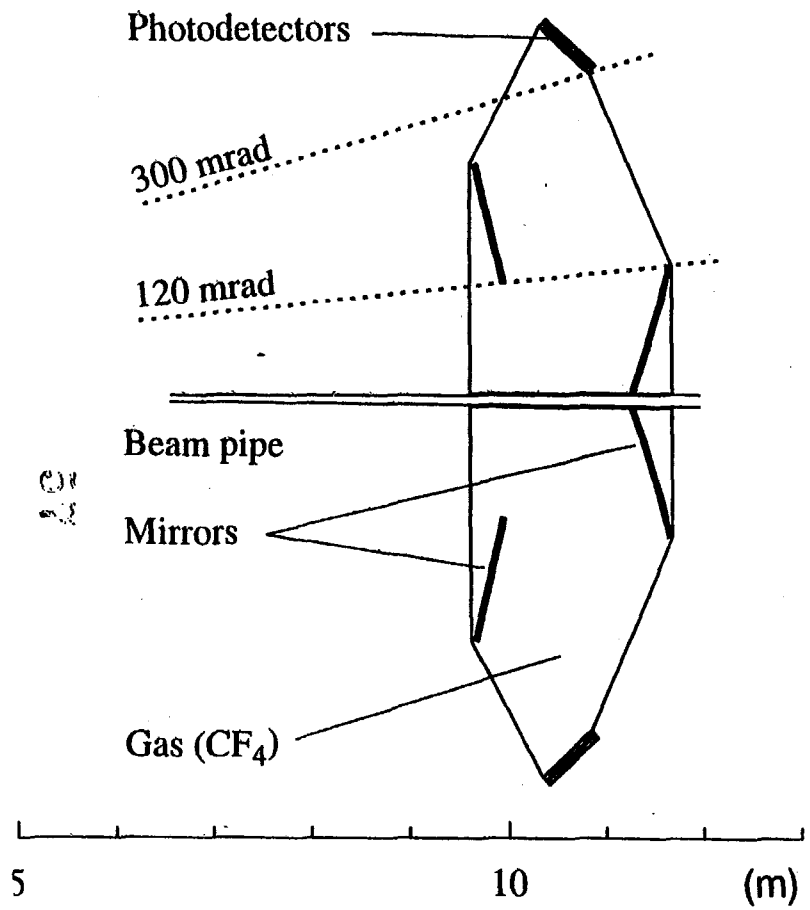
The LHCb detector



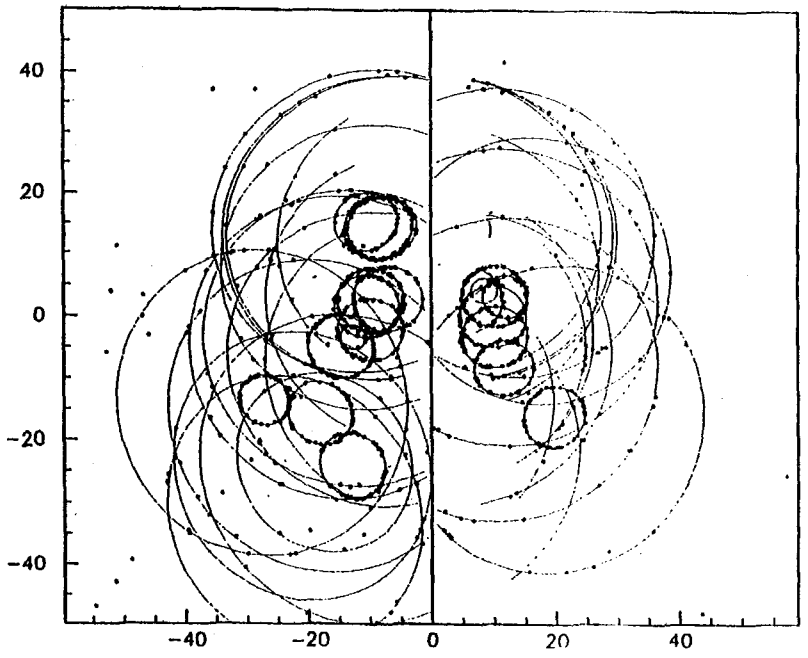
The RICH 1 counter



The RICH 2 counter



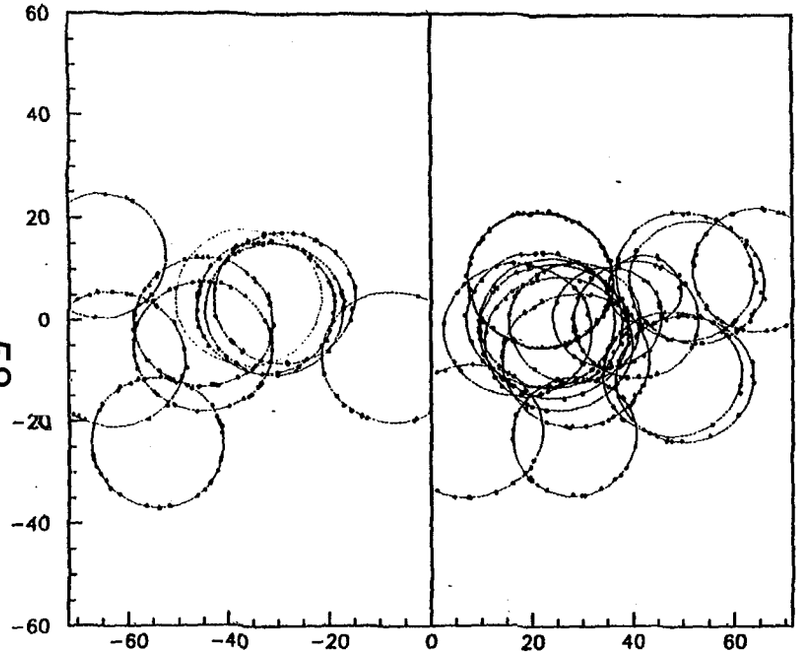
A simulated event in RICH 1



Contains $B_d^0 \rightarrow \pi^+\pi^-$

C_4F_{10} rings: 55 pe, ~10 cm Ø, $p_{th}(\pi)$ = 2.6 GeV/c
Aerogel rings: 15 pe, ~40 cm Ø, $p_{th}(\pi)$ = 0.6 GeV/c

The same event in RICH 2



CF_4 rings: 30 pe, ~20 cm Ø, $p_{th}(\pi)$ = 4.4 GeV/c

Overall system requirements

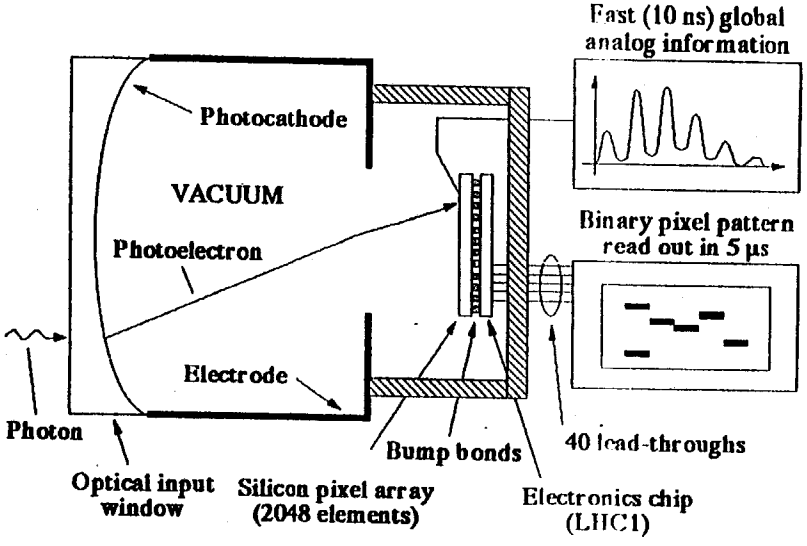
- **Photon detection**
  - RICH 1: 2 × (60 cm × 100 cm)
  - RICH 2: 2 × (72 cm × 120 cm)

    => ~2.9 m^2 total surface
  - Granularity: 2.5 × 2.5 mm^2
  - Active area coverage: 73 %
    => *~340'000 channels*
  - Single-photon sensitivity (λ = 200-600 nm)
- **Environment**
  - Radiation dose: 3 krad/year (RICH 1)
    1 krad/year (RICH 2)
- **Read-out**
  - Maximum occupancy: 8 % (RICH 1)
    1 % (RICH 2)
  - *LHCb-specific trigger scheme (see later)*
- **Photo-detector options**
  - *Pixel-HPD:* *cross-focussing geometry,* binary pixel readout (this talk)
  - Pad-HPD: "fountain" tube geometry, analogue pad readout
  - Multi-anode PMT: metal channel dynodes, analogue or binary readout

Motivations for pixel-HPDs

- **Features**
  - Past experience
  - Cross-focussed optics with kovar electrodes
  - Pixels bump-bonded to readout electronics
  - Binary read-out
  - Pixels
  - Vacuum tube compatibility
- **Performance**
  - ISPA-tubes + RD19
  - Good spatial resolution, robust to external E and B
  - Small capacitance (low noise, high speed), compact anode structure
  - Low power consumption (i.e. low heat dissipation)
  - Pattern recognition
  - Low outgassing, survives bake-out cycles

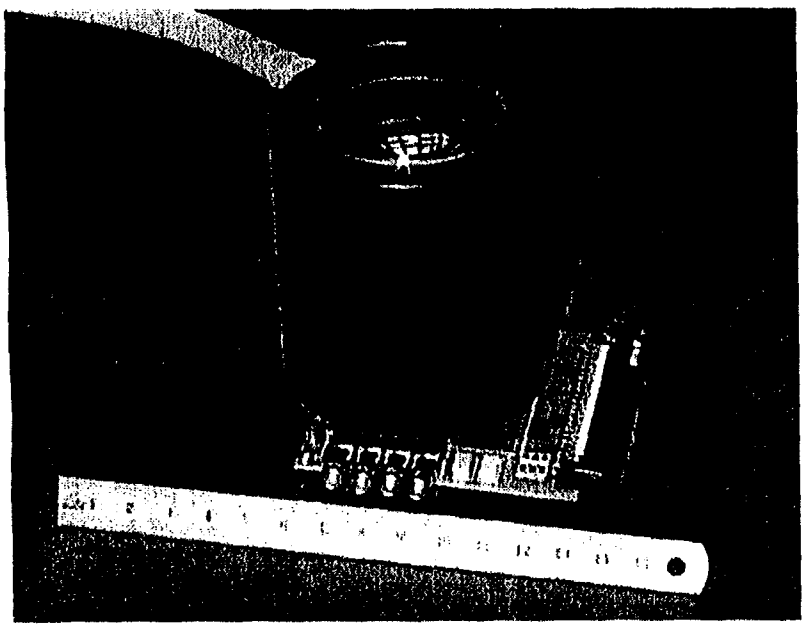
Half-scale prototype tube (schematic design)



40 mm active input diameter
11 mm active output diameter
4:1 demagnification factor
30 µm spatial resolution
20 kV accelerating potential (5000 e·h pairs)

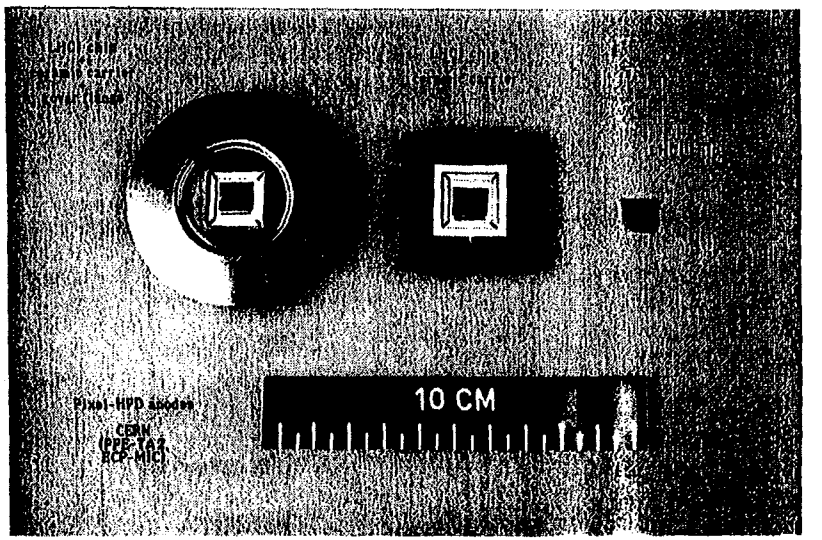
LHC1 electronics (see talk of E. Cantatore)

Half-scale prototype tube (photograph)

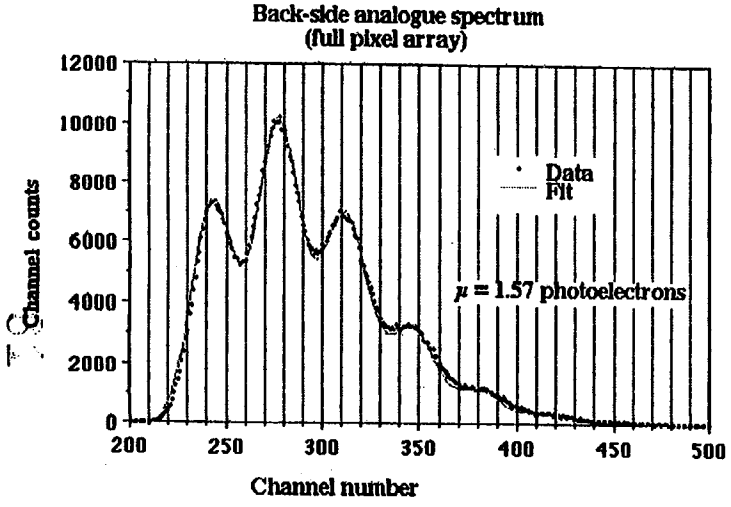


Manufactured by DEP B.V., Roden, The Netherlands

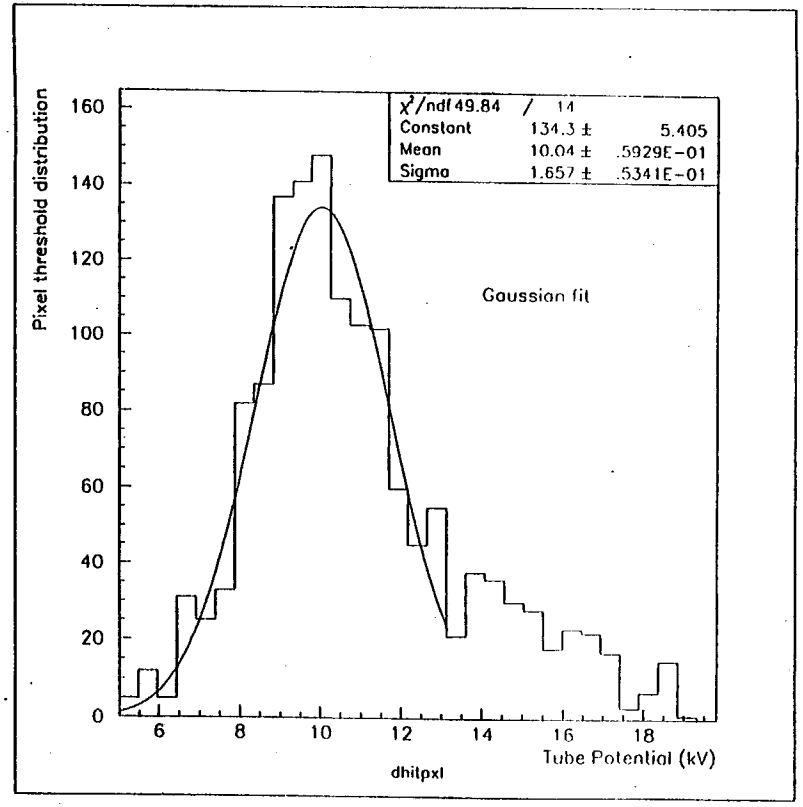
Half-scale prototype tube (anode assembly steps)



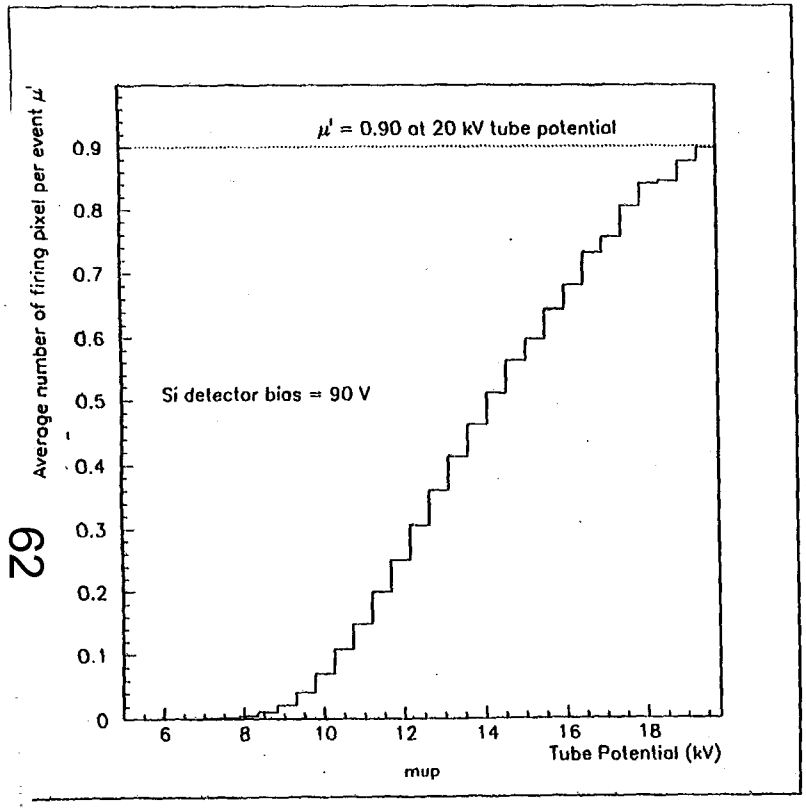
Back-side analogue spectrum



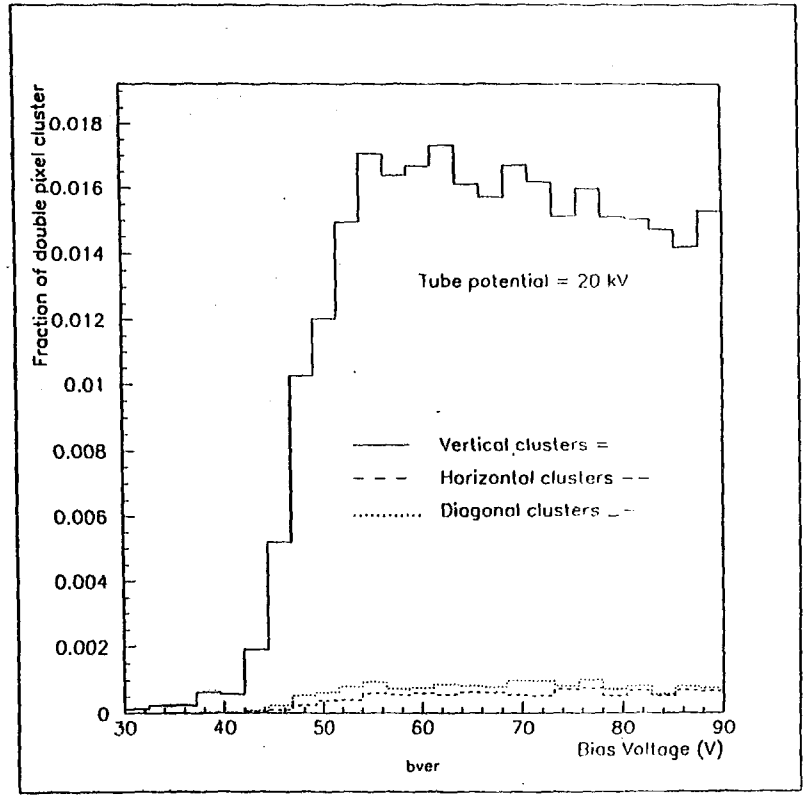
Threshold distribution



Firing pixels vs tube potential



2-pixel clusters vs det. bias



Single photo-electron detection efficiency

- Average number of pe μ (back-side analogue spectrum)
  - $\mu = 1.57$ pe
- Masked and inactive pixel correction (low or high thresholds)
  - 1456/2048 = 0.71
- Average number of firing pixels μ' (LHC1 binary readout)
  - $\mu' = 0.90$
- Single photoelectron detection efficiency
  - 0.90/(1.57*0.71) = 0.81
- Inefficiency attributed to:
  - photoelectron back-scattering at the detector surface (charge signal decrease)
  - charge sharing effects at the pixel boundaries (charge signal division)

Full-scale prototype tube

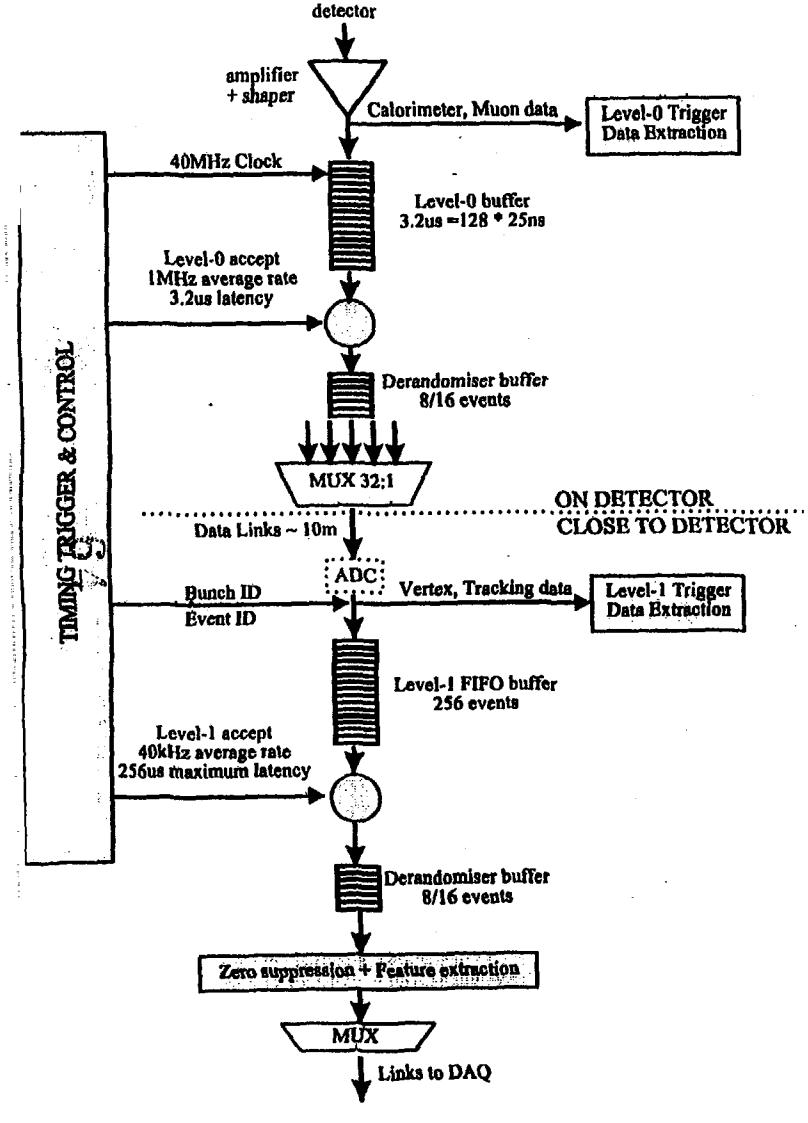
- Geometry
  - 72 mm active input diameter
  - 18 mm active output diameter
  - 4:1 demagnification factor
  - 100 μm spatial resolution

  => ~500 tubes for the entire RICH system
- First prototype
  - Phosphor screen anode
  - CCD readout

  => check of active area, electron-optics, magnetic field sensitivity.
- Second prototype
  - 61-pixels anode
  - UK RICH prototype readout

  => check of pe response to Cerenkov light

LHCb front-end architecture



Binary pixel front-end chip

REQUIREMENTS:

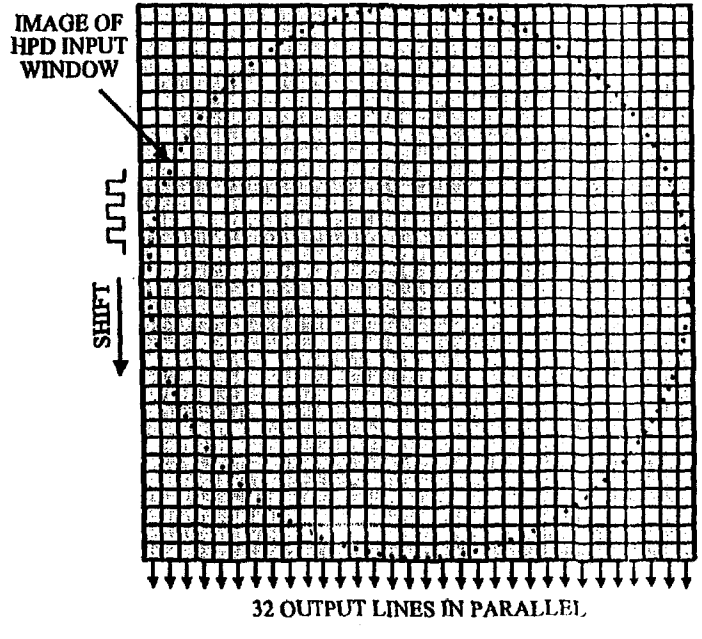
PIXEL DETECTOR & PIXEL ELECTRONICS CHIP PLACED INSIDE VACUUM OF HPD.
HIGH VOLTAGE OF 20kV => SIGNALS OF ~ 5000 e- PER PHOTOELECTRON

PIXEL SIZE DETERMINED BY GRANULARITY OF RICH DETECTOR AND DE-MAGNIFICATION OF TUBE

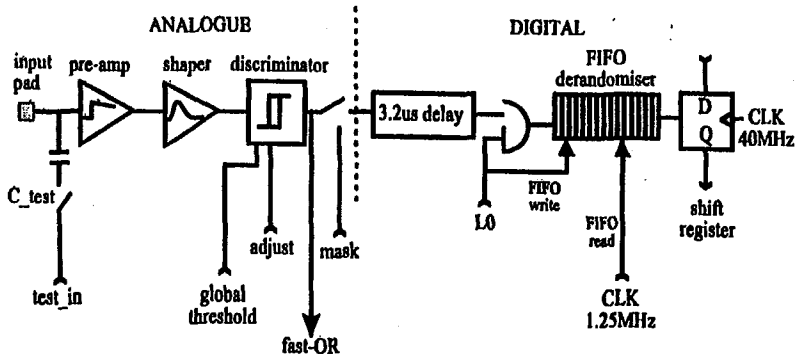
=> 32*32 MATRIX OF 500um*500um PIXELS

LARGE PIXELS: REDUCE CHARGE SHARING
RELAX CONSTRAINTS ON INTEGRATION OF ELECTRONICS
BUT INCREASE LOAD CAPACITANCE ON FRONT-END

EACH COLUMN CONFIGURED AS A SHIFT REGISTER FOR READOUT
@ 40MHz (32*25ns = 800ns => 1.25MHz)



Pixel cell



SPECS

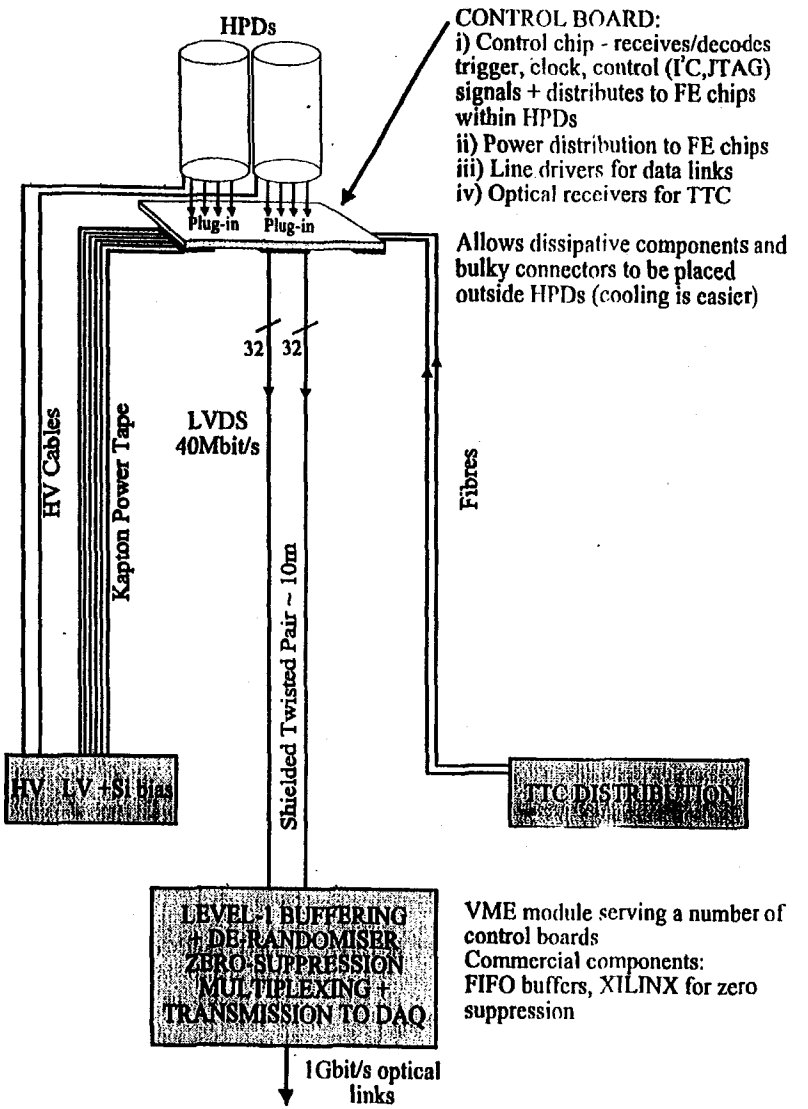
Analogue: Test input - test capacitors for system calibration
Pre-amp - DC-coupled to detector so must sink leakage current
Shaper - 25ns peaking time (tag hits with correct BX) with fast return to baseline
Discriminator - low threshold (2000e-), uniform (200e- RMS)
global setting + adjustment per pixel (current sources)
resets after 25ns
Fast-OR - OR of column/chip - advantage for chip testing
Mask - remove noisy/malfunctioning pixels

Digital: Delay - 3.2us, accurate to 25ns, store mutiple hits
analogue delay line of current-starved invertors is suitable if tuning circuitry is included
FIFO De-randomiser - depth for 16 triggers
input rate ~ 1MHz, output rate = 1.25MHz
16-bit RAM with sense amplifier
write & read pointers per column
Shift register - clocked @ 40MHz

Radiation Tolerant to 30kRad

Low power consumption < 100uW per channel

Interface, links and off-detector electronics



Current status and future plans for electronics

l Prototype HPDs successfully read out with LHC-1 electronics (100ns peaking time, mean threshold = 3000e- with 1000e- sigma)

l Reliability tests of chips inside vacuum following encapsulation within HPD
- do chips survive? (high temperature bake-out)
- do chips/detectors outgas? (contamination of photocathode)
- do bonds (wire and bump) survive?
Prototype HPD results are encouraging

l Implementation of circuitry in IBM 0.25um technology:
i) high density
ii) radiation tolerance - low threshold shift
iii) multiple metal layers - extra shielding
iv) small V_{dd} - lower power dissipation

l Additional radiation tolerance by using 'gate-enclosed' layout & guardrings

l Analogue front-end: ALICE pre-amp + shaper (see talk by Walter Snoeys) peaking-time/timewalk suitable for LHCb

l Discriminator: 1400e- threshold, 80e- RMS achieved on MEDIPIX chip ALICE design (see W.S.) is for 2000e- with < 200e- RMS

l Digital: adjustable delay line & FIFO de-randomiser designs underway

l Test structures of digital components to be submitted for fabrication by end of 1998.

l Design of full chip for LHCb to begin in 1999.

Conclusions

- **Half-scale prototype tube**
  - Electron-optics: behave as expected
  - Single-photoelectron response:
    - 80 % efficiency for active pixels
    - Inactive pixels due to tails in threshold distribution
  - Beam tests in June '98
- **Full-scale prototype tube**
  - Electron-optics design completed
  - Phosphor screen version in summer '98
  - 61-pixels version in autumn '98
- **Pixel front-end and readout electronics**
  - LHCb-specific front-end design underway
  - Readout implementation under study
  - Strong collaboration with Alice
  - Test chip submission by the end of '98

The BTeV pixel detector

Marina Artuso
Syracuse University
for the BTeV collaboration
PIXEL 98 WORKSHOP
Fermilab May7th, 1998

Introduction

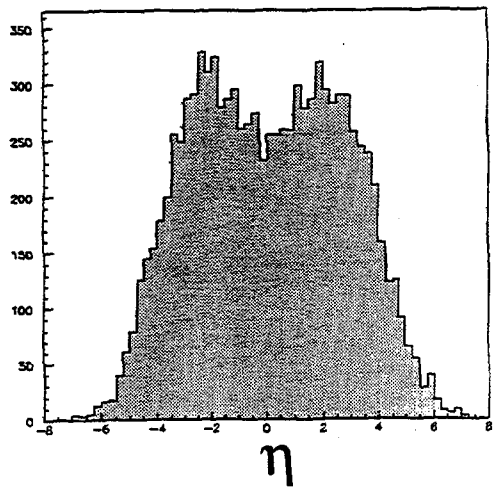
- BTeV's physics goals:
  - study b and c decays to
    - uncover phenomena beyond the Standard Model
    - measure CKM parameters
  - for example:
    - CP violating asymmetry in $B^0 \to \pi^+\pi^-$
    - CP violation and mixing in B_s decays

to achieve physics goals

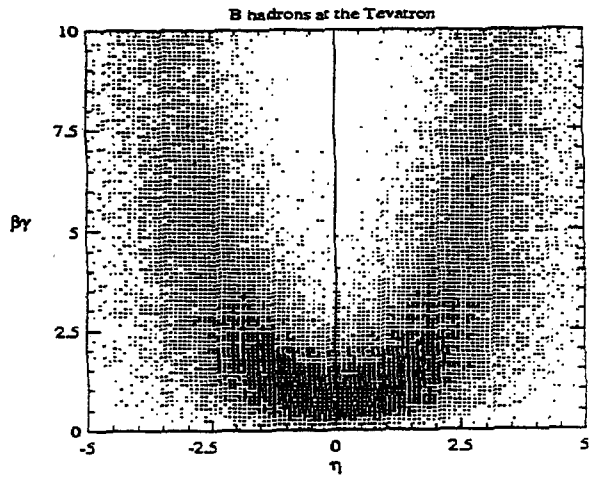
- pixel micro-vertex detector crucial for
  - tracking system - to achieve the vertex resolution and momentum resolution suitable for the physics goals (B_s studies and background rejection)
  - trigger system - detached vertex trigger in Level I, high efficiency for a variety of final states and flavor tagging options
- excellent particle id for π, K, p, μ ,e

Characteristics of hadronic b production

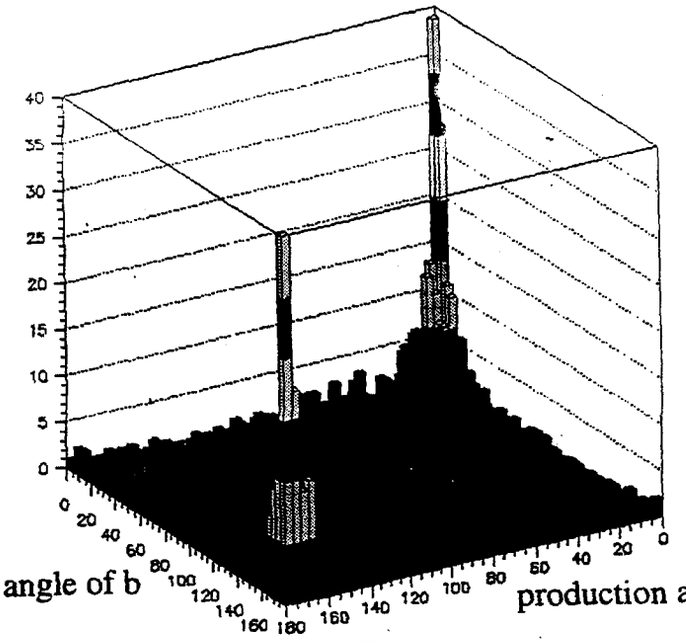
- b's produced "flat" in η, with $\langle p_t \rangle \sim m_h$



- The higher momentum b's are at larger η's (fig)



b $\bar{b}$ production angle correlation



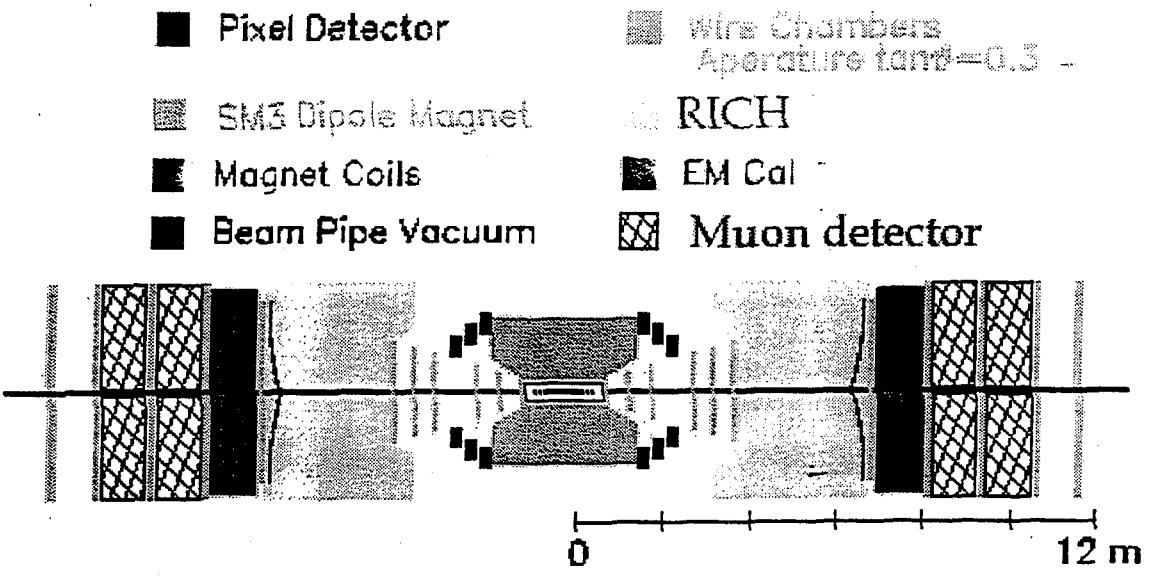
production angle of b

production angle of $\bar{b}$

The Tevatron as a b & c source

Luminosity (leveled)	$2x10^{32}$ cm^{-2}s^{-1}
b cross-section	100 μb
# of b's per 10^7 sec	$8x10^{11}$
b fraction	$2x10^{-3}$
c cross-section	>500 μb
Bunch Spacing	132 ns
Luminous region length	σ_z = 30 cm
Luminous region width	$\sigma_x \sim \sigma_y \sim 50$ μm
Interactions/crossing	<2>

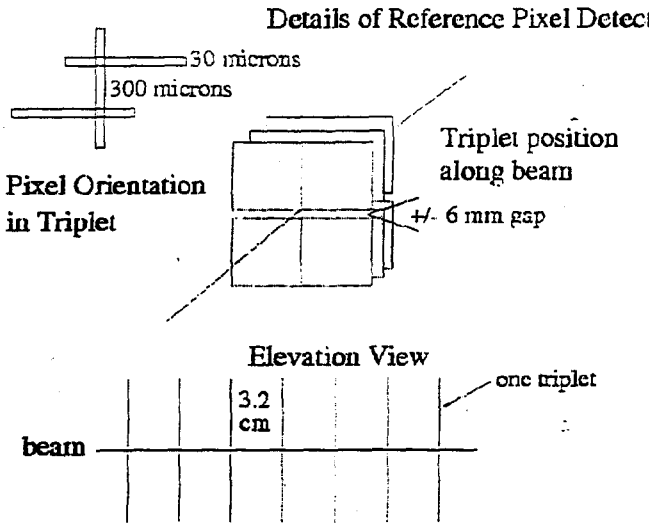
The BTeV detector



The Pixel Vertex detector

- Pixels necessary because we want to put detector as close as possible to beam. We have to fight radiation damage and detector occupancy problems. Expected dose ~8MRad/yr at 6 mm radius.
- System is inside vacuum pipe 6 mm from beam line. Distance is limited by radiation damage. (Done by P238 at CERN).
- Spatial resolution goal better than 9 μm

BTeV pixel detector geometry

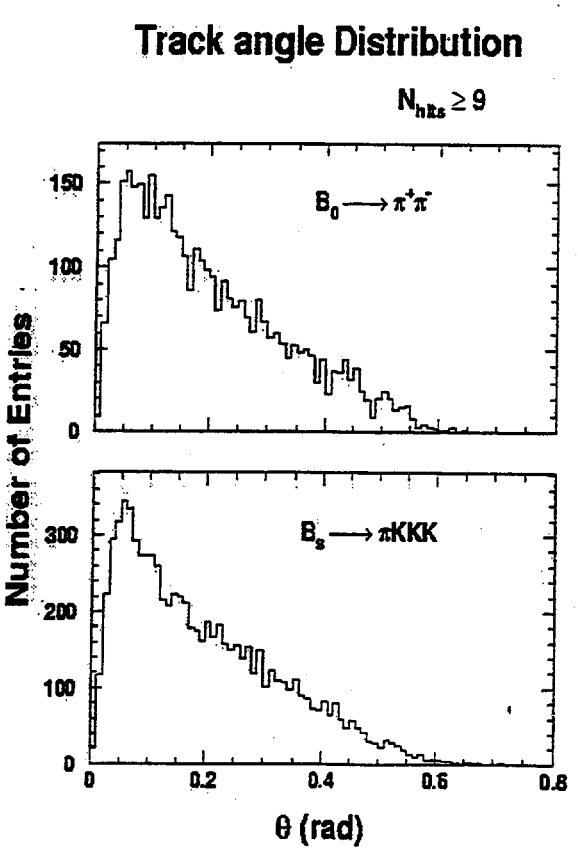


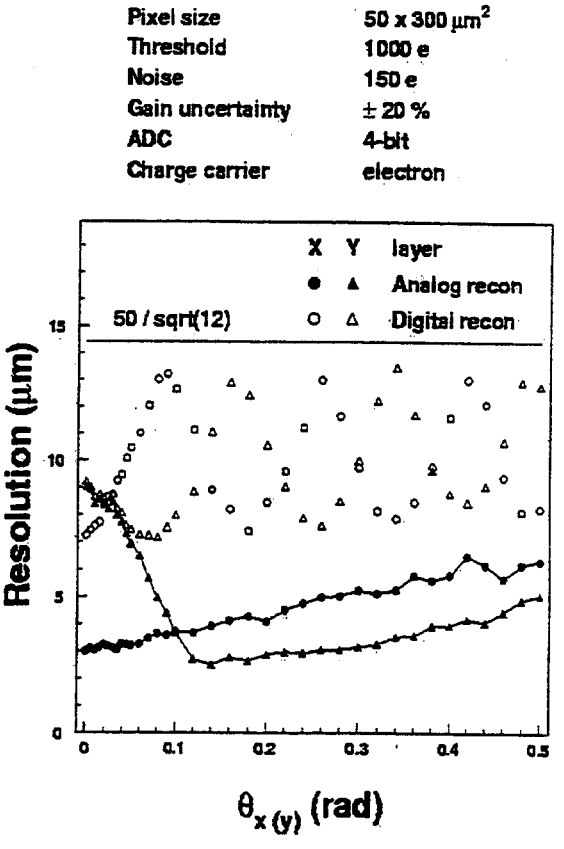
The pixel system

- Long detector system (93 planes along a 0.96 m distance along the beam line because of extended interaction region)
- Planes organized in triplet stations (three planes closely spaced) in order to provide a local slope, critical to our present trigger algorithm

Factors affecting the spatial resolution

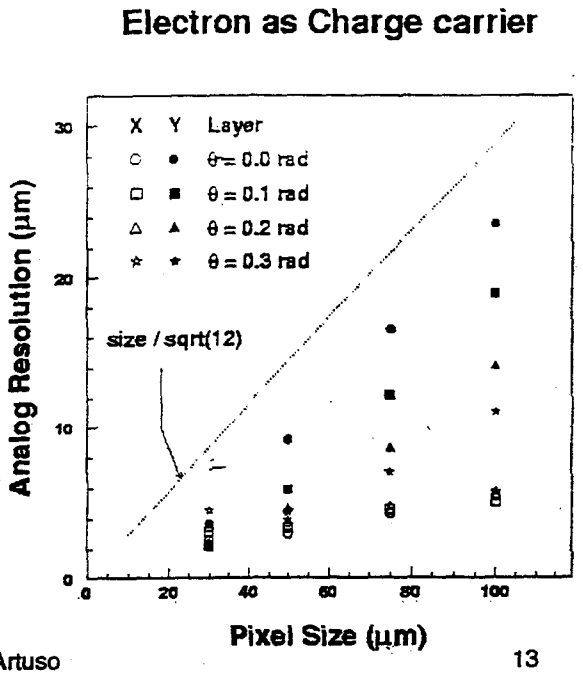
- Parameters affecting pixel resolution
  - pixel size
  - digital or analog electronics
  - threshold, adc bits, gain variations
  - electrons or holes as charge carriers (v_d 3:1 for electrons:holes)
- Factors affecting charge sharing
  - v x B effect
  - track angle





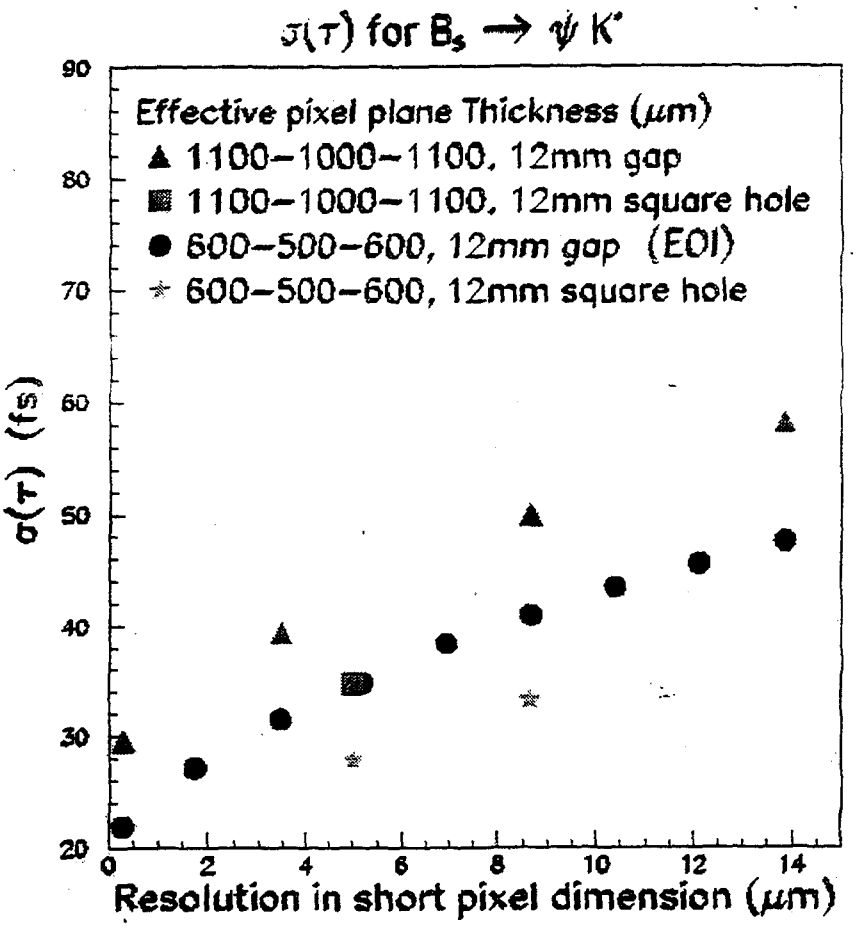
Results of pixel resolution studies

- Analog electronics gives average $\sigma <$ 5μm for 50μm pixel
- Alignment errors can be made not to dominate



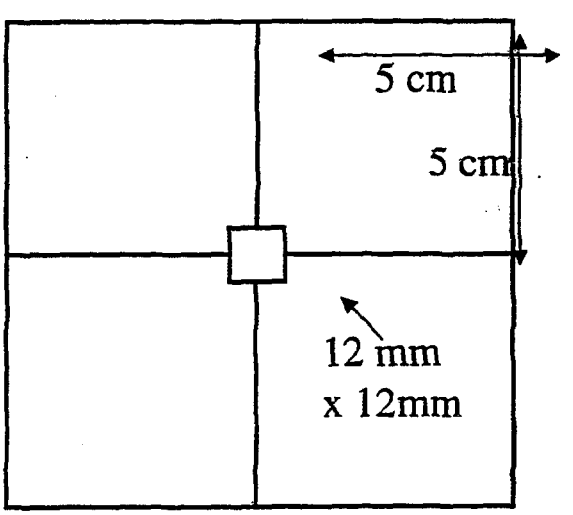
Factors affecting the time resolution

- There are two crucial techniques for reducing backgrounds: particle id & vertex resolution ≡ decay time resolution [$\sigma(\tau)$]
- How does $\sigma(\tau)$ depend on σ_x, detector material thickness and detector geometry?
- We have assumed 6 mm as minimum distance of detector to beam line, though 4 mm is what we calculate is safe (figs)



"Square Hole" pixel option

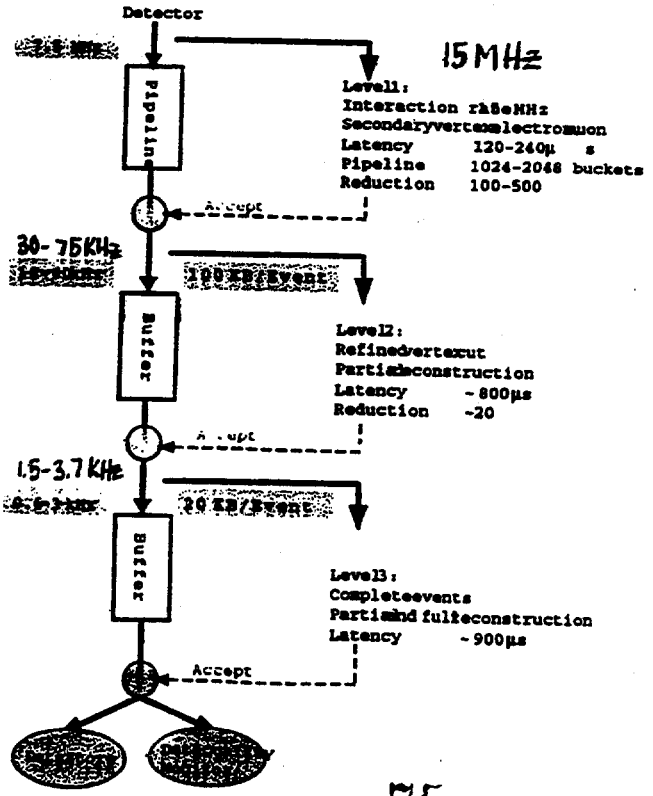
- Big Improvements possible by arranging detector to limit the gap:
- x_s reach



Readout system

- The baseline detector design dictates a system comprised of about 650,000 channels per plane (assuming a pixel size of 30μm x 500μm)⇔60 million in total
- average occupancy expected in the hottest chip (64 mm^2) is about 6 MHz at the maximum luminosity

BTeV data flow diagram

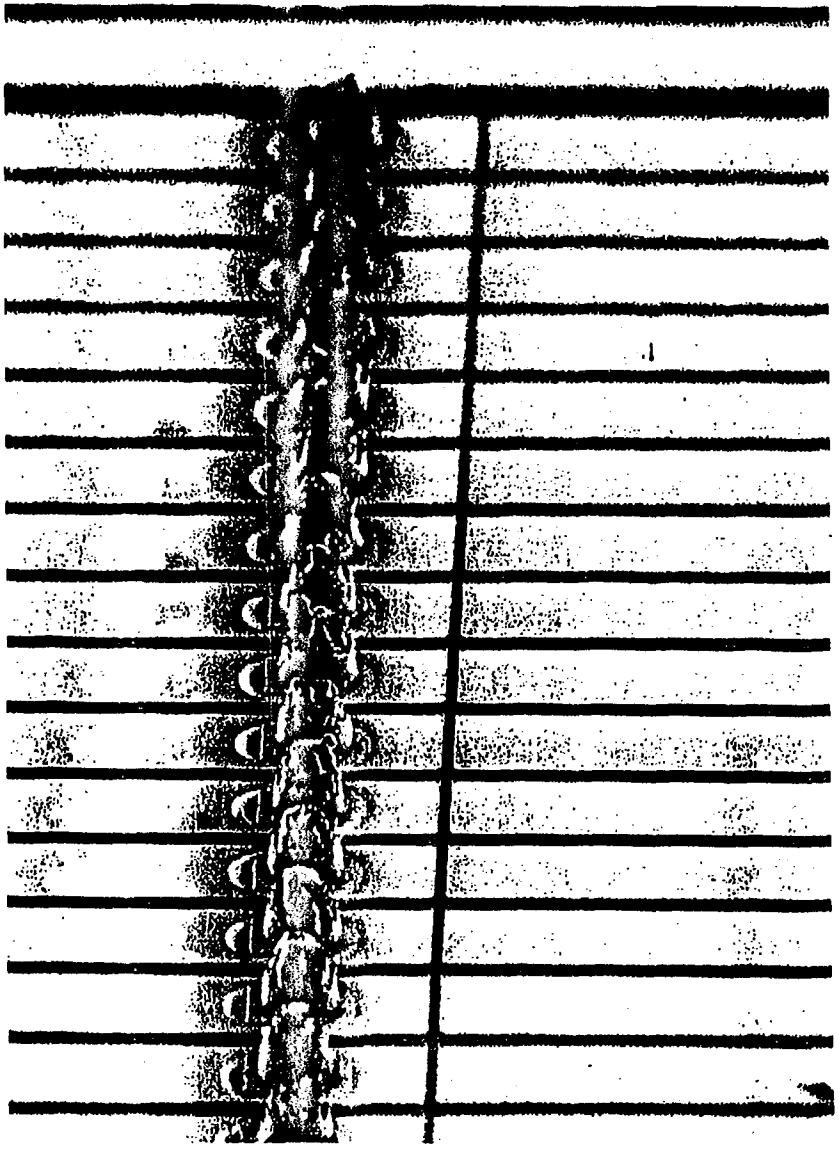


R & D plan: our challenges

- fine pitch bump bonding on a large scale system
- radiation hard components
- excellent readout electronics preserving the intrinsic low noise and low threshold performance in a complex system and with a data processing speed adequate for our needs ***(no information lost, trigger algorithm)***
- alignment accuracy consistent with the spatial resolution needed and with a retractable system
- low mass cooling and support structure

R & D stage I (1997- Spring 1998)

- Test of small prototypes of analog front end design stand alone and bump bonded to detector at the fine pitch considered for the final system (30-50 μm)
  - ✓**Indium bump bond of small readout chips to small detectors with pitches as small as 30 μm**
  - ✓**Evaluate performance of 2 different analog front end design**: FPIX0 (FNAL) and AIC501 (E. Atlas and S. Shapiro, tested at FNAL).



(PRB 2-2 Hong Kong Chip)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1				H								H	H			H
2				H O												
3		H														
4																H
5					H		H O									
6						N										H
7						H		N			H					
8															O	
9	H			D							H	H				
10													O*			
11																
12														H		N
13			H		H		H						O			
14															N	
15				H												
16																

N: not responding to test input
H: hot pixel
D: dead
O*: poor contact

5-not connected
20-hot
1- dead
4-not responding to input
28-bad one way or the other

R&D - stage II (1998-1999)

- Test of small detectors (~2cm x 2cm) bump bonded to full scale readout electronics (~1cm x 1cm).
  - →Prototype chip meeting BTeV specs
  - →Radiation hardness studies
  - →System issues associated with signal and power distribution
  - →large scale bump bond studies

R&D - stage III (1999-2000)

- Full scale module (1 sensor plane) to be used in BTeV system assembled
  - →Sensors bump bonded to readout electronics will be attached to the substrate providing mechanical support and thermal coupling to the cooling structure.
  - →Radiation hard technology
  - →Optimization in system design

R&D - stage IV (2000-2001)

- Full station assembly (triplet of planes closely spaced)
  - →Cooling system design
  - →Optimization of material budget
  - →Alignment procedure
  - →Full integration with trigger electronics

R&D - stage V (end of 2000-mid 2002)

- Full BTeV system prototype.
  - →Vacuum support
  - →Movable detector/readout relative to support
  - →Power supplies, regulation and voltage distribution
- This phase is the early part of the production!

Conclusions

- The pixel detector system is a crucial element in the BTeV tracking and triggering system
- Several challenges in the design of:
  - sensor
  - readout electronics
  - mechanical support and cooling system
- We have a detailed R&D plan, already under way